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Analysis of Quantization Noise and Power Estimation of Continuous-Time Delta Sigma Analog-to-Digital Converter Using Test Enable Feature For 4G Radios

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ABSTRACT

This paper presents a novel approach for completely test enable feature and low-voltage delta– sigma analog-to-digital (A/D) converters for cutting edge wireless applications. Oversampling feature of ADCs and DACs is enough to meet the requirement related to in-band and adjacent channel leakage ratio (ACLR) execution of 3G/4G portable radio. The quantization noise which is not filtered in ADC is addressed. We have achieved work power-optimization and test enable feature of oversampling ADC is uses in design and simulation so that the problem of quantization error in continues time sigma delta ADC is solved. This paper suggests support to designer for selecting appropriate topologies with various channel arrangements, number of bits and oversampling issues. A test enable feature of CT A/D is presented introducing the test signal generation (TSG) and the COrdinate Rotation Digital Computer (CORDIC) for evaluating the performance of ADC. This helps in addressing the challenge of 4G and upcoming 5G wireless radio. System level plan of a delta–sigma modulator ADC for 4G radios is studied.

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1. INTRODUCTION

Radio recurrence (RF) and mixed-signal topologies are fundamental components in future remote applications such as wireless 4G radios [1]. This type of innovation could enable the remote interchanges frameworks to relocate and help multiband and multi-standard radios, RF front-end/back-end, and advanced baseband systems. The drivers for mobile wireless communications are standards and protocols, frequency bands, power consumption, size, and cost [2].

This paper addresses the different issues in the design of future software radios 4G and 5G with emphasis on optimized power and test enable feature of oversampling analog- to-digital converters (ADCs) [3]. We have tried to review the challenges imposed on the wireless receiver design by the low-power specifications and small size in mobile terminals. The sigma-delta modulator structures that can conceivably be utilized for executing ADCs for portable remote radios are displayed in the point of view of a CMOS usage [4].

Generally, in modern luxury car, we have a cellular phone, fax, GPS receiver, television or even an internet browser in addition to radio. All these portable wireless communication systems use receivers to get the information signals from the world. The signals are received by an antenna, and the desired signal band, for example a GSM channel, is selected from the total received spectrum [5]. This frequency band undergoes analog filtering, amplification, frequency modulation and analog-to-digital conversion. Further signal

processing is done in the digital domain by a digital signal processor. Figure 1 shows Generic block diagram of wireless receiver which consists of an antenna, an RF/IF (Intermediate frequency) front-end, an ADC, and a digital signal processor (DSP) [6].

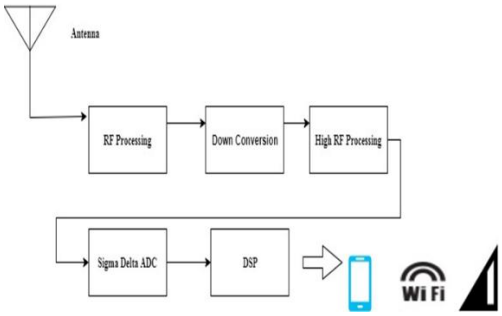

Figure 1. Generic Block diagram of Wireless Receiver

The ADC is used to digitize an RF, IF, or baseband signal depending on the receiver design. The location of the ADC in a receiver chain is very important that affects the overall performance, complexity, power dissipation, size, and cost [7]. The filtering and frequency translation are performed in digital domain, which reduces the complexity of the receiver and increases the flexibility. A flexible receiver consists of a digitally controlled analog front-end software-defined radio and a programmable digital back-end. The digital back-end forms the signals and feeds back control signals that reconfigures between different standards or dynamically within the same standard, the building blocks in the front-end. These blocks switch to a different set of performance values a different filter order or cut-off frequency for a filter, or a different gain and bandwidth for a low-noise amplifier, or a different gain for a variable gain amplifier, or different dynamic range and bandwidth for an ADC, etc [8]. Important tenors in the receiver design for wireless portable applications are: smaller product sizes, moderate products and longer stand-by times.

Products can be made smaller and cheaper by increasing the level of integration. Wireless communication has revolutionized everyone's lives by enabling a high speed connection directly to the people/information customers needs [12]. Wireless technologies such as 3G (third generation) and other such technologies coexist and work synergistically to meet customer needs. This requires different wireless systems that further needs multimode, multiband, and multi-standard mobile terminals. Sharing and/or switching building blocks is important requirement to extend the battery life and/or to reduce cost [9, 10]. Flexibility and adaptability are the key features in a multimode, multiband, and multi-standard wireless radio [11].

2. RESEARCH METHOD

2.1 System Level Modeling and Analysis of CT DSM Architecture as (DUT) for 4G Radio Application

Versatile sigma delta ADC configuration is shown in Figure 2, which consist of forward path coefficient b1, b2, b3 and integrator coefficient a1, a2, a3, a4 along with two digital to analog converter (DAC) DAC1 and DAC 2 and 2 bit quantizer for multi-mode structure in 5MHz, 7MHz and 10MHz channel information exchange limits. It is a reconfigurable and programmable ADCs which covers a perfect world an information exchange limit run to upgrade power and range for a specific application, by using the same ADC structures, re-use and plan strategies. Continuous time sigma-delta (CT ΣΔ) ADCs are used as a piece of remote correspondences, where a high information transmission at low power uses is required. Despite the fact that CT ΣΔ ADC offers the probability to change over high transmission limit data with a ridiculous low power usage. Table 1 gives the details about different modes of CT sigma delta ADC. In this table for wireless local area network (WLAN) in this mode feedback path (g1) and (g2) are connected and represented as dark straight line and similarly in Universal Mobile Telecommunications Service (UMTS)/Digital Video Broadcasting (DVB) (g1) feedback path trace is dashed line and (g2) feedback path trace line is dark straight line. Another mode of GSM (g1) feedback path trace and (g2) feedback path trace line is dashed straight line means unconnected. TABLE 2 shows delta sigma modulator performance and specification in 4 -G radios. In this table different parameter of CT ADCs such as Oversampling Ratio (OSR), Bandwidth (BW), Signal-To-Noise Ratio (SNR), modulation type and dynamic rang with variation of various mode of wireless along with CMOS technology is discussed.

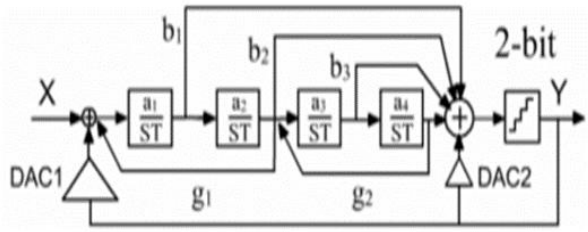

Figure 2. System Level Model of CT DSM Architecture for 4G Radio Application

Table 1. Different Modes of CT Sigma Delta ADC

MODE	(g1) Feedback path Trace	(g2) Feedback path Trace
WLAN	———————————	———————————
UMTS/DVB	------------------------	———————————
GSM	------------------------	----------------------------

Table 2. Delta Sigma Modulator Performance and Specification in 4 -G Radios

MODE	OSR	BW(MHz)	SNR (dB)	Estimated power and CMOS Technology	Modulation and dynamic Rang
WLAN	16	20	76	20 mW (130nm)	BPSK/64 QAM
DVB	25	4	54.6-56.5	19 mW (180nm)	BPSK/64 QAM
UMTS	12	1.92	65	3.5 mW (130nm)	BPSK/64 QAM
GSM	65	0.2	82	1.42mW (180nm)	BPSK/64 QAM

2.2 GUI of Noise Calculation CT Sigma Delta ADC Used for 4G Radio

There are different types of noise signals in the circuit affecting power and the errors are addressed by the system or circuit level techniques. This reduces the noise less than 25 percent of original present. When we calculate thermal noise and the clock jitter noise, it is around 75 percent of the total noise. GUI is designed for the noise calculation of the modulator. The delay is reduced or compensated by using a fast path around the quantizer which is used in the modulator. Using fully differential architecture is used; the mismatch in the rise and fall edge of the DAC output can be reduced. Figure 3 shows the results that are obtained after executing using MATLAB. For different values of all the parameters, different values of bandwidth and power are obtained as Lc , Nc and OSR.

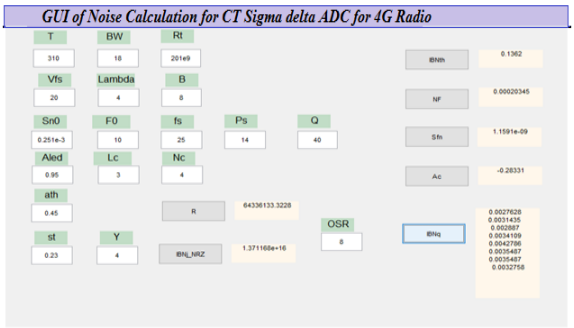

Figure 3. Noise Calculation for CT Sigma Delta ADC for 4G Radio

2.3 Power Consumption of CT Sigma Delta ADC used for 4G Radio

Figure 4 shows the power consumption of CT sigma delta ADC for 4G Radio. For the calculation of power consumption the different parameters are there on which the overall power consumption depends is represent in GUI block. The analog supply voltage plays a vital role in it for calculation of power in CT sigma delta ADC.

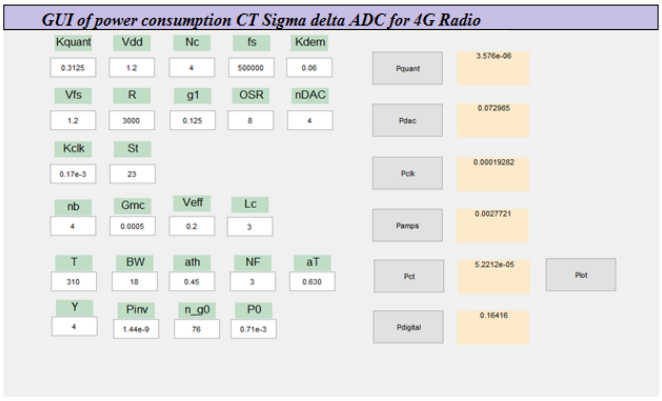

Figure 4. Power Consumption CT Sigma Delta ADC for 4G Radio

2.4 ∑-Δ Modulator ADC for Test Enable Feature for Wireless

A test enable feature of CT A/D is proposed introducing the test signal generation (TSG) and CORDIC for evaluating the performance of ADC to address the challenge of 4G and upcoming 5G wireless radio. System level plan of a delta-sigma modulator ADC for 4G radios is presented. Figure 5 shows block diagram of proposed ∑-Δ modulator ADC with test enable capability.

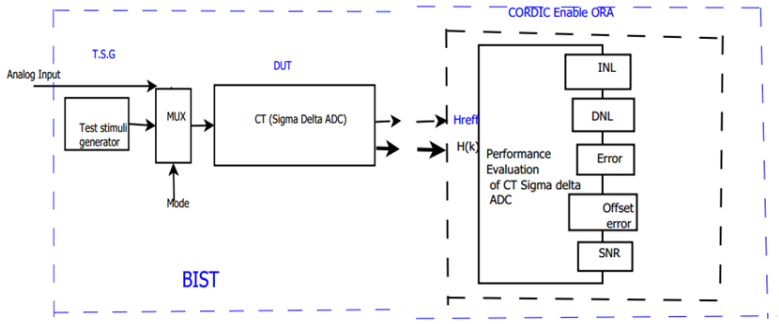

Figure 5. Block Diagram of Proposed ∑-Δ Modulator ADC with Test Enable Capability

2.5 Test Stimulus generation and power estimation of TSG

A simulink model of TSG is shown in Figure 6 which generates a sinusoidal signal which is required in subsequent stages of ADC as a test signal in ADC. Ramp signal is also required to test INL and DNL performance of ADC, which can be taken from test signal generated by TSG after converting in to ramp signal. Digital resolution based lossless (LDI) discrete integrator is used as TSG [2]. The resonators are obtained by cascading to integrator which, can be seen in Figure 6. The sinusoidal signal is generated while considering the variation in the coefficient a12 and a21 and the value of x1 and x2 fixed as $a21=2^{-6}$; $a12= 2.667\times10^{-4}$;x1(0) = 0 ; x2(0) = 0.0327159 and fos= 3.063MHz .

Power consumption of TSG is written as:

$$PTSG = 2\,P_{INT\_delay} + 2\,P_{Multiplier} + 2P_{Adder} \quad (1)$$

Where P_{INT_delay}=power of integer delay; $P_{Multiplier}$= power of Multiplier unit and P_{Adder}=power of adder unit.

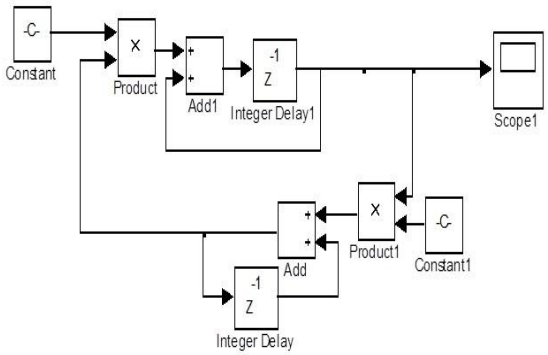

Figure 6. System Level Modeling of Test Stimulus Generator

2.6 Modeling and Analysis of Output Response Analyzer Using CORDIC Approach

Figure 7 shows block diagram of basic CORDIC technique ORA subsystem of test enable feature used to evaluate test parameter such as Integral Non-Linearity (INL) and Diffentail Non-Linearity (DNL) etc. There are several techniques for implementing ORA and based on complexity and bit resolution CORDIC used in the present work. CORDIC technique provides iterative formulation used to evaluate some elementary function, for example logarithmic, trigonometric and division. Reference histogram is obtained using CORDIC technique which consists of major components as a MUX, Embedded CORDIC calculator and resistor. Input offset error is calculated and final value of sine wave histogram is evaluated [11].

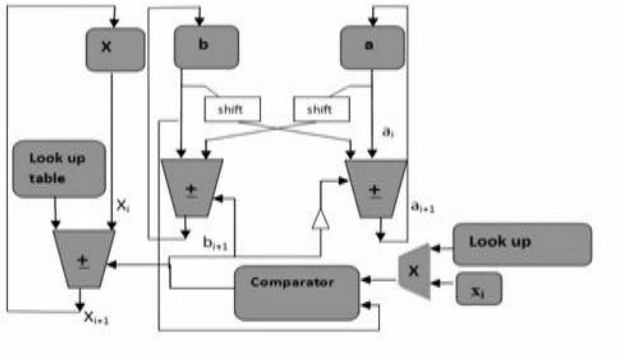

Figure 7. Block Diagram of Basic CORDIC Technique

Another component of CORDIC to calculate static parameter of sigma delta ADC such as DNL, INL, offset error and gain error. The dynamic parameters like Signal to Noise Ratio (SNR) are also calculated using this circuit. The values of DNL, INL, offset error and SNR affect the 4 G radio performance in wireless applications so that critical evaluation of this parameters are required.

3. RESULTS AND ANALYSIS

Table 3 shows extracted noise parameters of CT ADCs used for 4G radio which in Band Noise (IBN) is depends on choice of bits size, availably of Bandwidth (BW), order of modulator (Lc). Table 4 shows extracted power of CT sigma delta ADC which is technology depends on power supply (Vdd) and other parameter also for 4G radio. ADC works in different modes and in each mode power optimization is needed. The GUI based noise and power estimation is modeled to meet this requirement with enabling the test feature of ADC used in wireless receiver.

Tabulated result it is notice that minimum power dissipation Pct=3.06mw is achieved when Lc=3,Nc=4,OSR=10,BW=25 MHz.

Table 3. Extracted Noise Parameters for 4G Radio

S.No.	Lc	Nc	BW(MHz)	B(bit)	IBN_Th	IBN_NRZ
1.	4	3.2	18	12.5	0.113	0.242
2.	4	1	36	13.5	0.240	0.432
3.	3	4	25	12	0.365	0.480
4.	3	1	60	10.5	0.149	0.360

Table 4. Extracted Power of CT Sigma delta ADC for 4G Radio

S. No.	Lc	Nc	OSR	BW(MHz)	Vdd(Volt)	Pct(Author's work) (mw)	Pct (In this paper)(mw)
1	4	3.2	17.8	18	1.2	4	5.56
2	4	1	50	36	1.2	14.8	9.45
3	3	4	10	25	1.2	6.3	5.32
4	3	1	50	60	1.4	18.5	14.79
5	3	4	10	25	1.2	5.4	3.06

4. CONCLUSION

This paper discusses power productivity of various delta sigma modulator topologies used in wireless application. Power and noise estimation techniques are designed and simulated to exact the power utilization of the delta sigma modulator. The test enable features are modeled and simulated in MATLAB simulink environment for CT sigma delta ADC used in 4G radios. In this work quantization noise and other parameter are reduced significantly that were not addressed in similar research works.

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