International Journal of Informatics and Communication Technology (IJ-ICT)
Vol. 12, No. 3, December 2023, pp. 225~235
ISSN: 2252-8776, DOI: 10.11591/ijict.v12i3.pp225-235

2D router chip design, analysis, and simulation for effective communication

Prateek Agarwal[1], Tanuj Kumar Garg[1], Adesh Kumar[2]
[1]Department of Electronics and Communication Engineering, Faculty of Engineering and Technology, Gurukula Kangri (Deemed to be University), Haridwar, India
[2]Department of Electrical and Electronics Engineering, School of Engineering, University of Petroleum and Energy Studies, Dehradun, India

Article Info

Article history:

Received Oct 2, 2022
Revised Nov 28, 2022
Accepted Mar 4, 2023

Keywords:

Data packets
Field programmable gate array
Network on chip router
Simulation
Xilinx integrated system environment

ABSTRACT

The router is a network device that is used to connect subnetwork and packet-switched networking by directing the data packets to the intended IP addresses. It succeeds the traffic between different systems and allows several devices to share the internet connection. The router is applicable for the effective commutation in system on chip (SoC) modules for network on chip (NoC) communication. The research paper emphasizes the design of the two dimensional (2D) router hardware chip in the Xilinx integrated system environment (ISE) 14.7 software and further logic verification using the data packets transmitted from all input/output ports. The design evaluation is done based on the pre-synthesis device utilization summary relating to different field programmable gate array (FPGA) boards such as Spartan-3E (XC3S500E), Spartan-6 (XC6SLX45), Virtex-4 (XC4VFX12), Virtex-5 (XC5VSX50T), and Virtex-7 (XC7VX550T). The 64-bit data logic is verified on the different ports of the router configuration in the Xilinx and Modelsim waveform simulator. The Virtex-7 has proven the fast-switching speed and optimal hardware parameters in comparison to other FPGAs.

Corresponding Author:

Adesh Kumar
Department of Electrical and Electronics Engineering, School of Engineering
University of Petroleum and Energy Studies
Dehradun, India
Email: adeshmanav@gmail.com

1. INTRODUCTION

Network on chip (NoC) [1] has grown in prominence as various communication infrastructures have expanded. Other communication designs had been used in the past, but as core counts increased, these architectures turned out to be a bottleneck for upcoming systems on chips (SoCs) because they limited scalability, reusability, and difficulty. In the age of technology, the very large scale integration (VLSI) industry found a model known as SoC [2] and later uncovered many flaws in it, including underutilization of cores, low reusability, enormous complexity, and restricted scalability have been discovered a novel model termed NoC addresses the shortcomings of SoC. Individual effective on-chip communication design for SoC is called NoC. On a single chip, integrated circuits (IC) house multiple central processing unit (CPU) cores, memory, hardware cores, and analog components. In great capacity and high-end uses like aerospace, multimedia and defense, wireless, and wired communication schemes, these SoC are frequently employed [3]. Additional processors are uniting on a particular die as an IC technology scales and creating multiprocessor systems on chips (MPSoC).

The MPSoC technology is used to integrate complicated heterogeneous systems into a distinct chip and to allow on-chip communication. The processor elements of the MPSoC communicate using a variety of bus structures and communication methods. In terms of cost, performance, frequency of operation, and power requirements, the bus-based communication system is not a scalable architecture or a solution for future SoC design engineers [4]. The answer to the issues facing the semiconductor industry is NoC, which can meet the increased transistor packing density, cost, greater operating frequency, performance, and shorter time to market.

NoC is the system version of MPSoC that has been confirmed to be a unique and effective method for utilizing interconnections, and it inter-exchanges data among numerous nodes unified on a distinct chip. In the design of an NoC architecture, topology, switching, and routing techniques are critical. The NoC can be built and organized using different topologies in terms of the core and router computer architecture, as well as the processes required to implement the flow management, switching, and routing strategy. Data flow control is concerned with the quantity of data transportation or strength in the channels and routers. Routing is a methodology for defining the greatest pathway for the data and messages from the communicating device to the proposed end or the receiver. The two dimensional (2D) mesh NoC is a typical NoC architecture due to system scalability and the use of a simple routing approach. Long-distance traffic, on the other hand, may have severe broadcast dormancy. According to Pang *et al.* [5], star-type NoC has been used for long-distance transportation to pass through a second-level network. In the design of a NoC, the routing procedure is the content of the network layer. It is the most important factor that affects NoC network communications.

Small area communication or local area networks (LAN) are found to be suited for 2D-NoC architecture, whereas big area networks are not. The higher number of nodes can be considered while conducting a study as part of this ongoing endeavor. When transferring data across nodes, additional features like data security through encryption and decryption can be used. If we can combine system safety measures with via-node data transmission, it will be appropriate for broad communication systems and wireless data transfer. Every electronic device nowadays, from a little mobile phone to a satellite, contains SoC. The SoC has evolved quickly throughout time and is still processing information quickly. However, the devices are scaling down quickly because of the tremendous growth of the semiconductor industry. As a result, today's SoC is communication-centric. However, due to their inability to keep up with the rate at which devices are being scaled down, the present bus designs, which consist of wires for worldwide interconnection in SoC scheme, are experiencing proposal emergencies. NoC is a developing pattern that is quickly rising to the top of the competition to replace traditional bus designs as a reaction to this crisis.

The difficulty of SoC communication integration on-chip die is one that the NoC design and field programmable gate array (FPGA) implementation must overcome. With the continual reduction in chip dies size, the likelihood of failure in NoC is rising [6]. A fixed NoC can become irregular as a result of arbitrary placements, which may also impair the uniformity of actual topological design. Since throughput, area, power, and latency are the four most important factors in chip design [7], the intercommunication between the many cores and intellectual property (IP) modules on a single chip may have an impact on the device's communication and system performance [8].

The problem statement of the work is to design the hardware chip for the 2D router for communication using different ports and analyze the performance on different FPGAs for effective communication. Most of the work is done to synthesize the chip parameters on the FPGA board. The research work examines the performance of various FPGAs to assist chip designers in selecting the FPGA that has the best hardware and timing performance. The organization of the manuscript is as follows: section 2 details the related work, and section 3 presents the research method. The results and discussions are given in section 4, followed by the conclusions in section 5.

2. RELATED WORK

The work on the 2D NoC router has been focused on mesh topological NoC (4×4). The NoC nodes are addressed using the XY routing approach [9]. It is one of the most essential strategies for addressing nodes and routing data packets between nodes or processing elements inside NoC. The NoC design was formed with the very high-speed IC hardware description language (VHDL) programming language and simulated with the Xilinx 14.2 and Modelsim software. The logic routing and synthesis were done on the Virtex-5 FPGA [10] for 8-bit, 16-bit, 32-bit, 64-bit, and 128-bit data transmission across nodes in the NoC which was properly configured and implemented. FPGA synthesis settings were assessed by the hardware parameters and completely reported using the hardware report synthesized for the NoC chip. The 5-port optical router was detailed [11]. The chip design was focused on mesh and ring topological network modeling, simulation, and synthesis. The cluster size was regarded as (2×2), (4×4), (8×8), (16×16), (32×32), (64×64), (128×128), and (256×256) for 2D NoC router design [12]. The projected design decreased the

quantities of data frames navigated for long-distance communication, according to simulation results. The performance was gained of 17.2% and 10.3% respectively for standard 2D mesh and level 2 mesh topologies and provided by (12×12) star type NoC. When the network grows larger, the star-type NoC's performance improves still more while consuming less space and power. The star-type NoC future work will be included the development of novel routing algorithms and system designs for adaptive routing in arrange to better balance traffic loads and get better overall performance.

Different studies have been done related to NoC design for different routing approaches, as well as a system-based NoC simulator [13]. The core concept of the NoC simulator, design, and settings was detailed for the test strategy of NoC system planning. The investigation was done for the additional on-chip routing strategies, such as a novel linear programming (LP) routing strategy. The local traffic showed a significant improvement in performance for NoC systems, according to the findings. It was identified that LP routing can handle locality traffic without causing conflict in nearly a third of the cases. If the network system has excessed resources for sharing, such as connections, and channels, and the immediate rate of flit production is less than or equal to the volume for accepting flits, LP routing is more successful. The simulations of application-specific NoC topologies for audio video (AV) benchmark, MPEG-4 decoder, and applications demonstrated that regular NoC outperforms irregular NoC systems in the terms of performance. The simulation was following eight digital signal processing (DSP) connectivity architectures in a chip topology. The fundamental NoC concept and architecture are used to configure the topology structure in which distinct routing node architecture was followed for arbitration, routing, and data packet format. Moreover, (2×4) interconnection architecture was designed based on routing node coding, routing algorithm, and node degree routing direction. The work was carried out using active-HDL software programming and simulation. The data can continue to function without interruption to increase data transfer efficiency. After synthesis, the maximum frequency can reach 268 MHz, which can be utilized as a benchmark for the next research. Kumar *et al.* [14] focused on the architecture and network interface (NI) design performance examination and evaluation. This research is based on a 2D 4×4 topology 2D mesh. On the NIRGAM simulation, we compare the packet latency and throughput of the two algorithms using the XY and odd-even (OE) routing algorithms, respectively. NIRGAM is a software tool based on system 'C' and a cycle-accurate behavior simulator that provides the platform to realize the routing algorithms and NoC applications for different topologies. The findings show that for the XY routing algorithm, the packet delay in the X-dimensional direction is greater than the packet delay in the Y-dimensional direction and the X-dimensional path has higher average throughput. The packet delay in the X-dimensional direction is lower than in the Y-dimensional direction and the X-dimensional direction's average throughput is roughly equivalent to the Y-dimensional direction. To determine if the algorithm is good or terrible, the average throughput to average packet latency ratio is used. The better the performance, the higher the ratio. The results show that the OE routing method has a ratio of 2.5358, whereas the XY routing algorithm has a ratio of 2.1126. As a result, the OE routing method performs better in the 2D mesh topology [15].

Hardware chips are used to implement the 2D, 8×8, and 16×16 mesh topological networks. The ability to spot faulty nodes and replace them is the programmable structure's main benefit. The X and Y axis crossbar address generation mechanism can be used to identify problematic nodes. The device utilization findings indicate a 2% change in the number of slices, a 1% change in the number of slice flip-flops, a 1% change in the number of 4 input look-up tables (LUTs), and a 1% change in the number of bonded input/output blocks (IoBs) when the NoC cluster configuration changes from an (8×8) to a (16×16) NoC. For both networks, the amount of memory used is 58,820 kB and 71,466 kB, respectively. Small-area communication or LAN networks are found to be suited for 2D-NoC architecture, whereas big-area networks are not. The higher number of nodes can be considered while conducting a study as part of this ongoing endeavor. When transferring data across nodes, additional features like data security through encryption and decryption can be used. If we can combine network security methods with node data transfer, it will be suitable for wireless data networks and long-distance communications [16]. In response to this dilemma, the emergent paradigm of NoC is rapidly winning the race to supplant conventional bus designs. To address varied chip design requirements and routing techniques, numerous NoC topologies have been created. Regular-size processing devices can be included on a single chip with a mesh topology. Additionally, compared to other routing protocols, it is much easier to create and implement different routing protocols into it. Therefore, crossbar architecture has been created in VHDL and simulated in Xilinx ISE 14.1 to use the Xilinx XC5VLX30-3 FPGA to evaluate the operation of NoC on hardware [17]. Routers are based on the wormhole switching principle. Round-robin routing is used to create routers on FPGA platforms. The suggested router confronts the FIFO status of input ports during each clock cycle and the priority of each input port is constantly adjusted. The architecture described above makes sure that each input port is treated fairly. Utilizing Xilinx tools, the proposed architecture was created in VHDL. The design's functionality has been confirmed and its implementation in ISE design suite 14.1 has been completed.

The flat tree NoC architecture, supported by eight nodes at the root, was reported in the study. The performance of the system was assessed using the Virtex-5 FPGA, xc5vlx20t-2-ff323 device. Several test cases are used to experience the design. The data flow for the same cluster setup is seen on the Modelsim waveform. Additionally, the FPGA's timing and hardware support settings are examined. The architecture is scalable and modular in design. It can be used to create a massive tree in which several nodes can communicate with each other through their parents and root nodes [18]. The upcoming study may focus on network security techniques and their integration with NoC configurations for big clusters [19]. When the rotator on chip (RoC) or ring NoC chip has been created and modeled in Xilinx 14.2 software, Modelsim 10.1 b software is used to functionally simulate it. A data packet's intercommunication is confirmed when it reaches its destination and the NoC chip can link to up to 6,553 nodes. With FIFO logic integrated, a token ring concept is used to indicate the priority of communicating nodes at the same instance. Node addresses are utilized to identify the nodes and Xilinx synthesis results are used to determine hardware attributes such as the number of logic gates, LUTs, memory use, and the minimum-maximum times required to route packets [20]. The Virtex-5 FPGA is used to validate the results through data transfer between nodes. The outcomes show a superior option to currently used ring setup up structures. To create a ring topological network's programmable and adaptable structure, a large amount of work has been put into NoC design and FPGA synthesis. Future configurations of the same structure could include more nodes. Additionally, the concept of cryptographic techniques for encryption and decryption can be used to move data between nodes. Modelsim 10.0 software with 8, 16, 32, 64, and 128-bit data transfer successfully replicates the functionality of the 3D multilayer mesh NoC design produced in Xilinx 14.2 using VHDL. The performance hardware and time parameters are also assessed for mesh nodes with cluster sizes of (2×2×2), (3×3×3), and (4×4×4). The selection of the node effectively utilizes XYZ routing and addressing. The created chip works at a 735.00 MHz frequency. For larger networks like wireless sensor networks, the scalable design establishes inter-node communication. It is also concentrated on the integration of network security into hierarchical NoC architectures with multilayer systems environments.

Machine learning models [21] for multiple NoC topologies synthesized on Vitex-5 FPGA for various cluster configurations are constructed and validated. The described NoC structure may be advantageous for future MPSoC that seek high performance and fault tolerance from their communication topology. The programmable structure is a reconfigurable MPSoC solution that permits online configuration and guarantees that minute faults do not affect system performance. Mesh NoC is scalable and based on XY routing [22]. When comparing the two, the ring NoC has wider coverage. The parent-child (root) memory architecture and optimal routing technique form the basis of the tree NoC architecture. The design is more reliable for NoC and reconfigurable telecommunication networks and more suited for mobile signaling technologies like SS7. Modelsim 10.1b is used to verify data transfer while the resulting design is tested on an FPGA for the various test scenarios. Data on hardware usage, such as the number of slices, flip-flops, input LUTs, bounded IoBs, and gated clocks (GCLKs) used to implement the design, are included in the synthesis report that is generated. In Xilinx ISE 14.7 and Modelsim 10.0, the study project effectively builds 2D mesh (4×4) and 3D mesh (3×3×3) NoCs. The nodes in the 2D and 3D mesh NoC are addressed using the XY and XYZ routing. FPGA is a scalable device that offers a synthesis environment with various NoC cluster sizes. The FPGA is set up with a mesh topology structure that allows 2D mesh (16×16) and three dimensional (3D) mesh (8×8×8) designs with 256 nodes capable of communication (N=2, 4, 8, 16, 32, 64, and 128, respectively). Timing parameters and hardware resource usage are crucial factors for semiconductor businesses. The simulation work presented in the manuscript, will help NoC designer to estimate the resources utilization before developing the actual device by taking into consideration the known hardware design aspects, memory utilization, and timing factors to produce large-scale NoC.

3. RESEARCH METHOD

The data packets are transferred and communicated by the router. It is happening using the networking device that performs the traffic direction over the communication network. The data packets are sent over the networks to get effective communication such as in optical fibers, telecommunication, and high-speed switching [23]. The design of a 2D network route is shown in Figure 1 in which the 2D router is configured using the East_data_input, West_data_input, North_data_input, South_data_input, and Local_data_input. The corresponding outputs are East_data_output, West_data_output, North_data_output, South_data_output, and Local_data_output respectively for the inputs.

The data flow in packets is shown in Figure 2. This is bidirectional communication and the data communication mechanism is based on packet switching [24] and the flow control for NoC applications [25]. The data input to the crossbar switch is through all 5 ports defined for east, west, north, south, and local direction and corresponding outputs using the control module. The objective of the flow control is to use the

effective reasons for the maximum throughput and good performance that depends on the channel bandwidth and buffering capacity for the allocated network. In switching the flow control is maintained as bufferless using several ports. The quality of the source is maintained by the throughput of the network. The arbiter is also used to decide which switch port needs the process in the crossbar switch [26]. The router is used in different sensor networks [27] and wireless communication technologies such as ZigBee [28] technology.

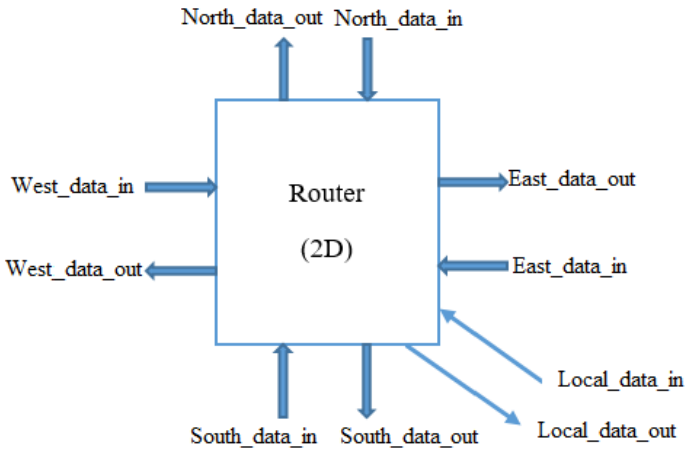

Figure 1. 2D NoC router [23]

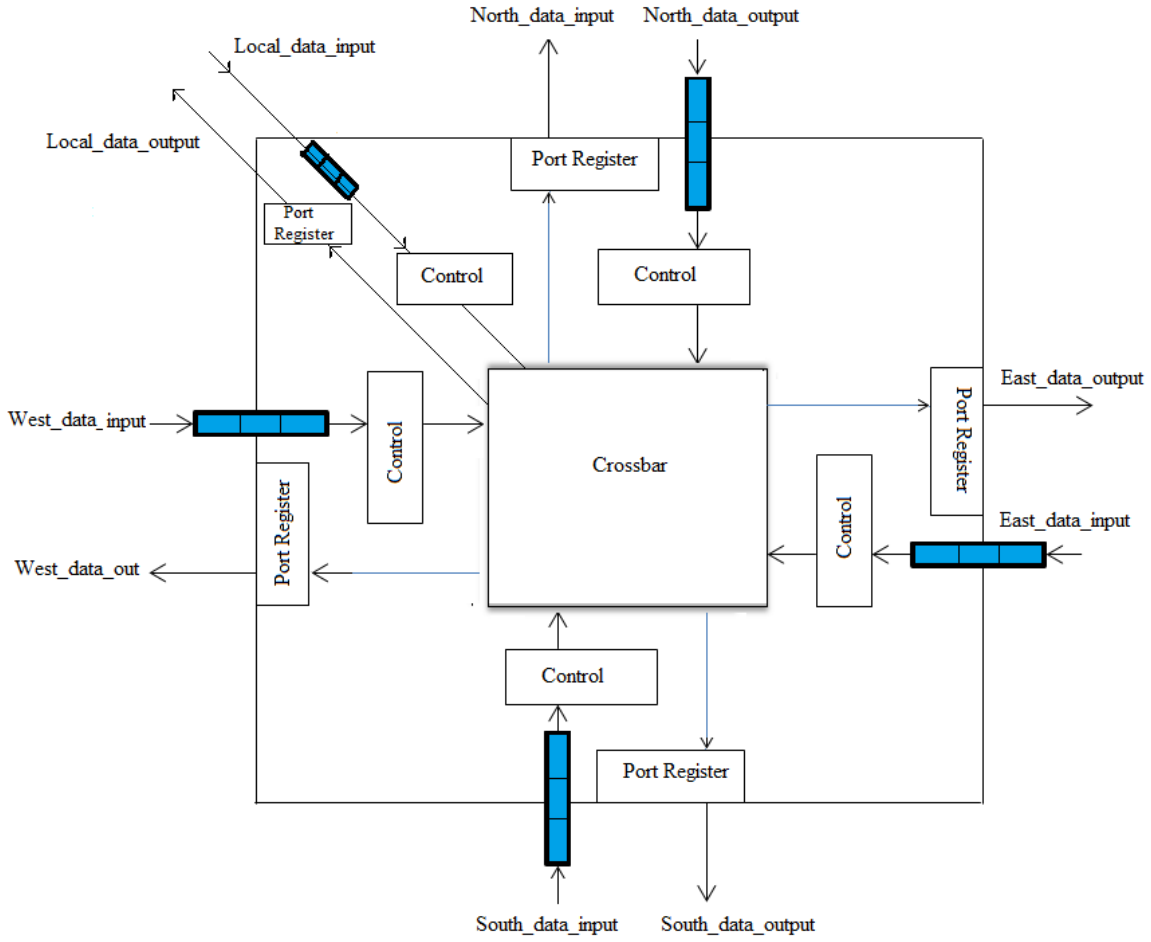

Figure 2. NoC router data packets transmission

4. RESULTS AND DISCUSSION

The chip design of the 2D-NoC router is done in Xilinx ISE 14.7 and depicted in Figure 3. The register transfer level (RTL) detail and pins functionality is given in Table 1 which provides the compressive use and application in the design strategy. The internal schematics of the design are also given in Figure 4. The Modelsim simulation waveform for the router functionality of 64-bit data communication is verified for the test inputs given. Figure 5 shows the router's waveform simulation using different binary ports. Figure 6 shows the waveform simulation of the router using different ports in hexadecimal. Figure 7 shows the waveform simulation of the router using different ports in the American standard code for information interchange (ASCII).

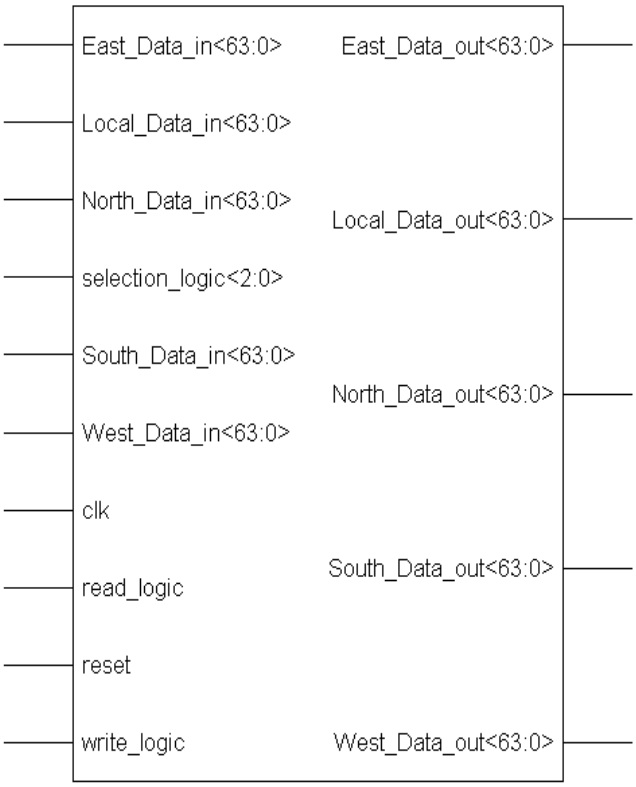

Figure 3. RTL of the chip design

Table 1. Pin functions of the chip design

Pins	Function
East_data_in <63:0>	It uses the input port to offer 64-bit data packets input (east direction)
West_data_in <63:0>	It uses the input port to offer 64-bit data packets input (west direction)
North_data_in <63:0>	It uses the input port to offer 64-bit data packets input (north direction)
South_data_in <63:0>	It uses the input port to offer 64-bit data packets input (south direction)
Local_data_in <63:0>	It uses the input port to offer 64-bit data packets input (local direction)
Clk (1-bit)	It uses the 50% duty cycle clock input signal to provide the rising edge of the clock
reset (1-bit)	It provides the input signal to reset the data input/output port values and corresponding latches
East_data_out <63:0>	It uses the output port to offer 64-bit data packets output (east direction)
West_data_out <63:0>	It uses the output port to offer 64-bit data packets output (west direction)
North_data_out <63:0>	It uses the output port to offer 64-bit data packets output (north direction)
South_data_out <63:0>	It uses the output port to offer 64-bit data packets output (south direction)
Local_data_out <63:0>	It uses the output port to offer 64-bit data packets output (local direction)
Read_logic (1-bit)	It is the control input used to write the contents from different ports into registers
Write_logic (1-bit)	It is the control input used to read the contents of different registers into ports

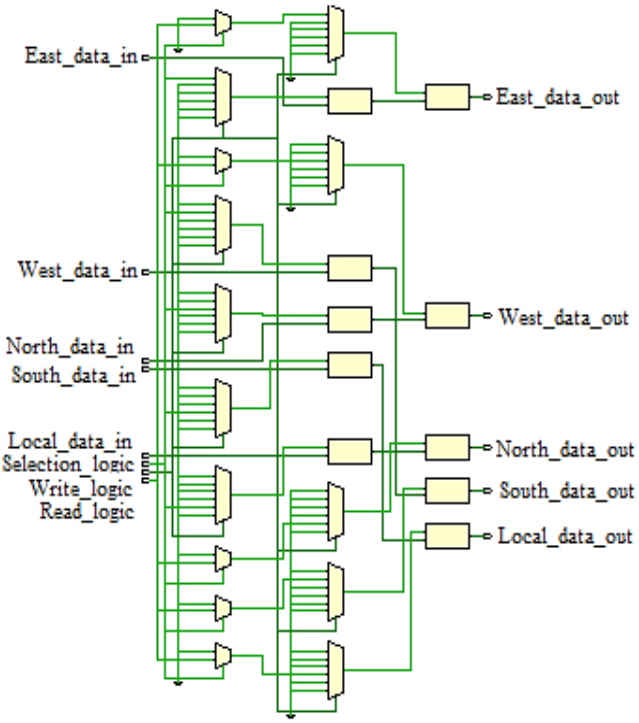

Figure 4. The internal schematic in Xilinx of the 2D router design

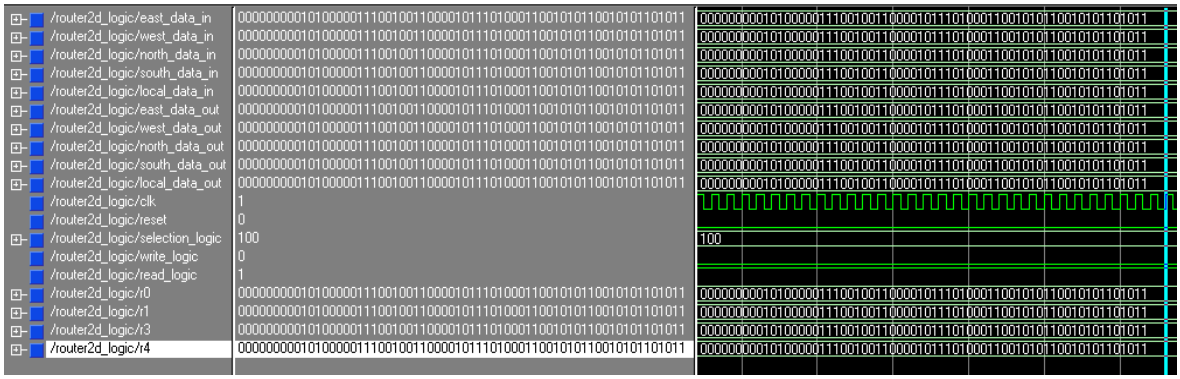

Figure 5. Waveform simulation of the router using different ports (in binary)

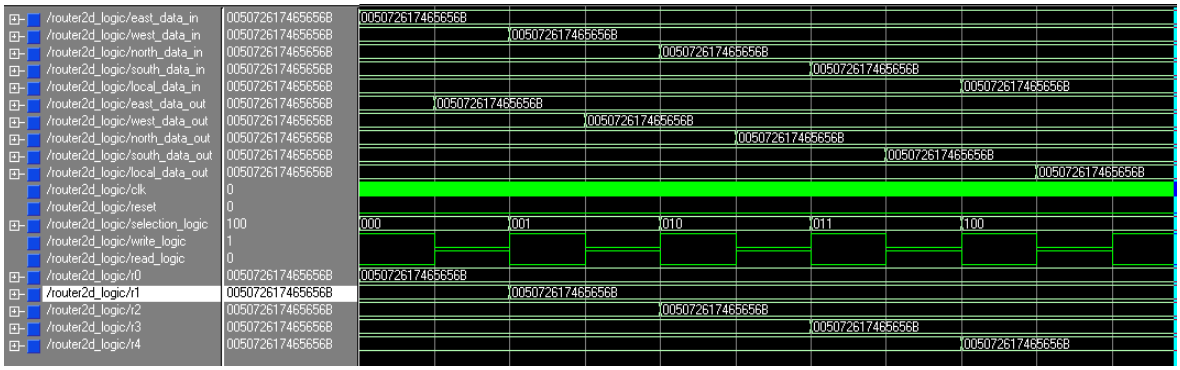

Figure 6. Waveform simulation of the router using different ports (in hexadecimal)

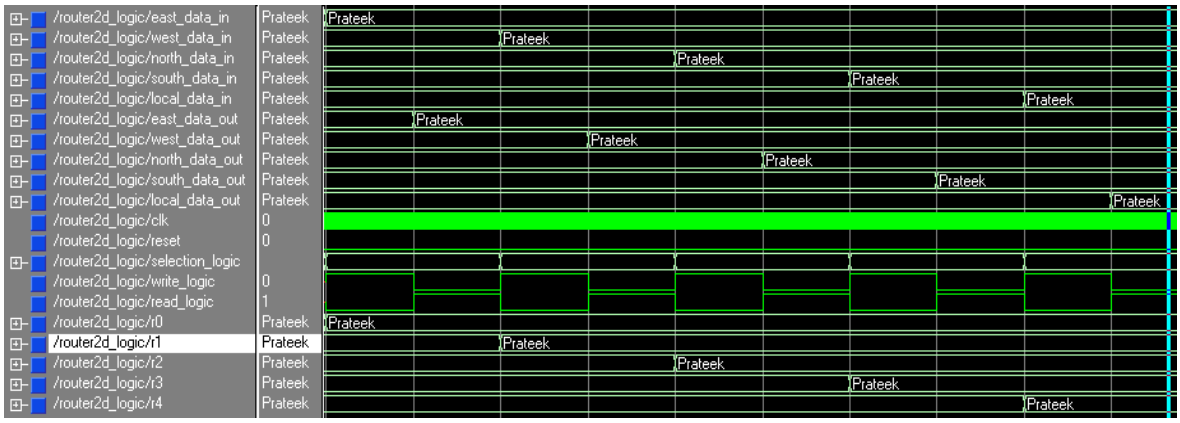

Figure 7. Waveform simulation of the router using different ports (in ASCII)

The simulation input and outputs in the waveforms are East_data_in <63:0>=01010000 01110010 01100001 01110100 01100101 01100101 01101101 (binary)=1'h5072617465656B (hex), West_data_in <63:0>=01010000 01110010 01100001 01110100 01100101 01100101 01101101 (binary)=1'h5072617465656B (hex), North_data_in <63:0>=01010000 01110010 01100001 01110100 01100101 01100101 01101101 (binary)=1'h5072617465656B (hex), South_data_in <63:0>=01010000 01110010 01100001 01110100 01100101 01100101 01101101(binary)=1'h5072617465656B (hex), Local_data_in <63:0>=01010000 01110010 01100001 01110100 01100101 01100101 01101101(binary)=1'h5072617465656B (hex), write_logic='1', read_logic='0', the selection_logic changes from "000", "001", "010", "011", and "100" for different ports respectively. The output of the ports is obtained when write_logic='0', and read_logic='1'. The data on the ports is verified as East_data_out <63:0>=01010000 01110010 01100001 01110100 01100101 01100101 01101101 (binary)=1'h5072617465656B (hex), West_data_out <63:0>=01010000 01110010 01100001 01110100 01100101 01100101 01101101 (binary)=1'h5072617465656B (hex), North_data_out <63:0>=01010000 01110010 01100001 01110100 01100101 01100101 01101101 (binary)=1'h5072617465656B (hex), South_data_out <63:0>=01010000 01110010 01100001 01110100 01100101 01100101 01101101(binary)=1'h5072617465656B (hex), Local_data_out <63:0>=01010000 01110010 01100001 01110100 01100101 01100101 01101101(binary)=1'h5072617465656B (hex).

The hardware parameters summary on different FPGAs is listed in Table 2. The timing values of the design on different FPGAs are listed in Table 3. Figures 8 and 9 show the variations against the obtained results of the FPGA resources for hardware and timing utilization.

Table 2. Different FPGA resources as hardware parameters summary

Hardware parameter	Spartan-3E (XC3S500E)	Spartan-6 (XC6SLX45)	Virtex-4 (XC4VFX12)	Virtex-5 (XC5VSX50T)	Virtex-7 (XC7VX550T)
Slices	368	184	368	184	184
Slice flip flops	640	320	640	320	320
LUTs	326	10	326	326	10
IOBs	647	647	647	647	647
GCLKs	5	0	5	5	0

Table 3. Different FPGA summary in terms of timing parameters

Timing parameter	Spartan-3E (XC3S500E)	Spartan-6 (XC6SLX45)	Virtex-4 (XC4VFX12)	Virtex-5 (XC5VSX50T)	Virtex-7 (XC7VX550T)
Minimum period (ns)	1.894	0.951	0.971	1.187	0.170
Minimum input arrival time before clock (ns)	4.502	1.838	4.471	1.969	0.339
Maximum output required time after clock (ns)	4.137	3.648	3.892	3.044	0.669
Maximum combinational path delay (ns)	6.031	4.600	4.863	4.231	1.178
Maximum frequency (MHz)	50.00	275.00	400.00	290.00	515.00

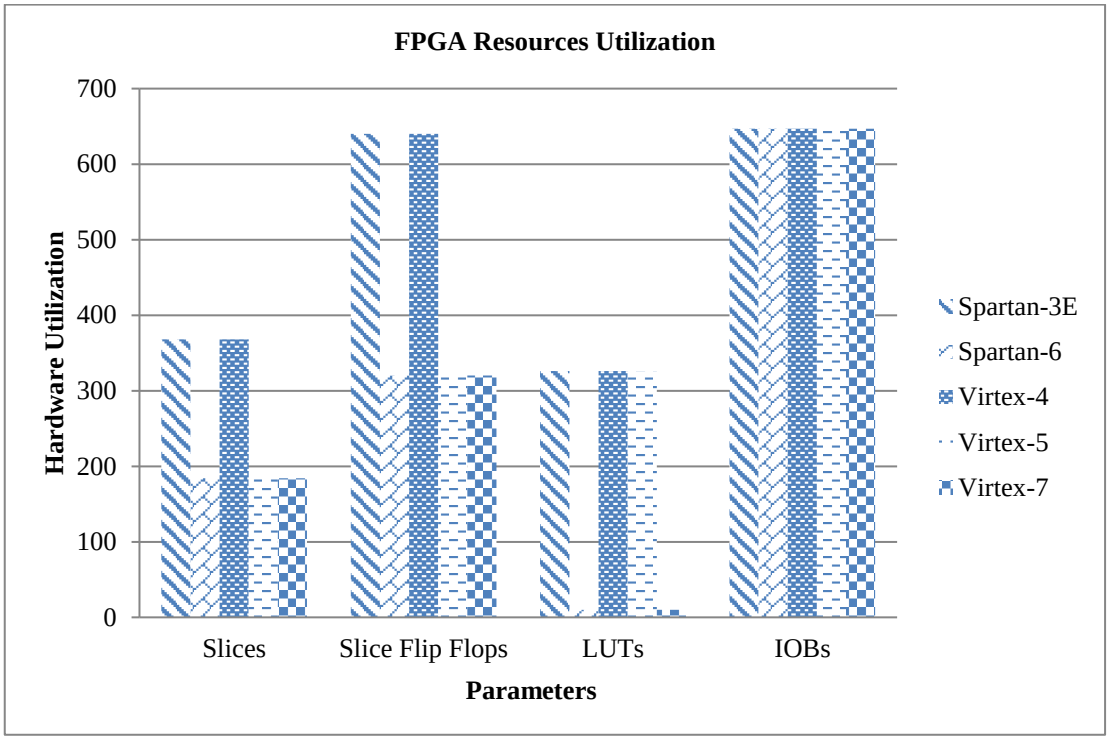

Figure 8. FPGA resources utilization summary

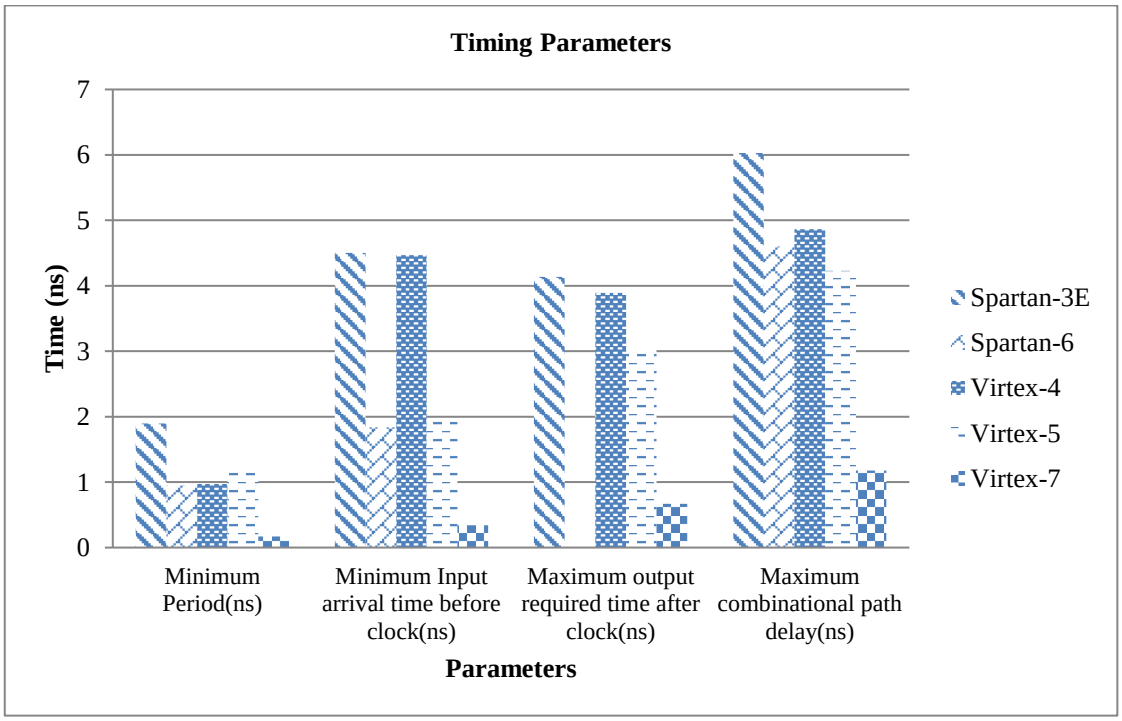

Figure 9. FPGA timing parameters utilization summary

5. CONCLUSION

The router transmits the data over the network. Routers use data packets, which can contain a variety of messages, files, data types, and simple transfers like online engagement, to route and guide network data. The hardware chip design and simulation of the 2D router are done successfully in Xilinx ISE 14.7 and Modelsim software. The chip design is verified using the different test inputs in which the 64-bit and

communication are verified using test cases on different input/output ports of the router. The behavior is verified on the different FPGA hardware such as Spartan-3E (XC3S500E), Spartan-6 (XC6SLX45), Virtex-4 (XC4VFX12), Virtex-5 (XC5VSX50T), and Virtex-7 (XC7VX550T). The comparative study presents that slices are 368, 184, 368, 184, and 184 respectively for different FPGAs. The slice flip-flops are 640, 320, 640, 320, and 320 respectively for different FPGAs. The number of LUTs is 360, 10, 326, 326, and 10 respectively for different FPGAs. It has been identified that the frequency support for different FPGAs is Spartan-3E (50.00 MHz), Spartan-6 (275.00 MHz), Virtex-4 (400.00 MHz), Virtex-5 (290.00 MHz), and Virtex-7 (515.00 MHz). The mining values indicate that the Virtex-7 FPGA has the optimal timing values in comparison to other FPGAs and Virtex-7 shows maximum frequency support for the router chip design.

ACKNOWLEDGEMENTS

Thankful to the VLSI Design Lab, University of Petroleum and Energy Studies, Dehradun, India for providing the simulation facility.

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BIOGRAPHIES OF AUTHORS

Mr. Prateek Agarwal is B.Tech. in Electronics and Communication Engineering from Uttar Pradesh institute of Technology, (UPTU), Lucknow India in 2006. M.E. in Electronics and Communication, Thapar University (TU), Patiala India in 2008. Pursuing Ph.D (Electronics and Communication Engineering) in the domain of VLSI design. His areas of interest are VLSI design and digital communication. He has published 5 research papers in international and national conferences. He can be contacted at email: prateek.aggrawal@gkv.ac.in.

Dr. Tanuj Kumar Garg received B.Tech. in Electronics and Communication Engineering from G.B.P.U.A.T, Pantnagar, Uttarakhand in 2000, M.E from Delhi College of Engineering, Delhi in 2001 and Ph.D. from Uttarakhand Technical University, Dehradun, Uttarakhand. He is currently working as Assistant Professor in Department of Electronics and Communication Engineering, Faculty of Engineering and Technology, Gurukula Kangri (Deemed to be University). His research interest includes microstrip antennas, reconfigurable antennas, metamaterials, metamaterial antennas, tunable antennas, leaky wave antennas, and VLSI design. He can be contacted at email: tanujkgarg@rediffmail.com.

Dr. Adesh Kumar is working as a senior associate professor in the Department of Electrical and Electronics, Engineering ‘‘University of Petroleum and Energy Studies, Dehradun, India. He is B.Tech. in Electronics and Communication Engineering from Uttar Pradesh Technical University Lucknow, India in 2006. M.Tech (Hons) in Embedded Systems Technology, from SRM University, Chennai in 2008. Ph.D. (Electronics Engineering) form University of Petroleum and Energy Studies (UPES), Dehradun India in 2014. He has also worked as senior engineer in TATA ELXSI LIMITED Bangalore and faculty member in ICFAI University, Dehradun. His areas of interest are VLSI design, embedded systems design, telecommunications, and signal processing, He has published more than 100+ research papers in international peer-reviewed journals (SCI/Scopus) and conferences. He is the reviewer of many SCI/SCIE and Scopus journals such as IEEE Transactions of Industrial Electronics, Wireless Personal Communications, Microsystem, Technologies, 3D research, Springer, Journal of Electronic Science and Technology, Journal of Visual Languages and Computing, Elsevier, World Journal of Engineering, and Emerald are few of them. He has supervised 7 PhD scholars and 5 candidates are doing research under his supervision. He has chaired more than 10 sessions at international conferences and is involved in the Ph.D. evaluation committee at UPES, India. Guest Editor: Special Issue-"Intelligent devices and computing applications" in Computer Systems Science & Engineering, Journal, Tech Science, 2022 (SCI Indexed). Guest Editor: Special Issue-"Intelligent communication and smart grid automation applications" in Intelligent Automation & Soft Computing, Journal, Tech Science, 2021 (SCI Indexed). Editor: Proceedings of intelligent communication, control, and devices in advances in intelligent system and computing (AISC), book series, Springer, vol. 989, 2020 (Scopus Indexed). He can be contacted at email: adeshmanav@gmail.com.