International Journal of Informatics and Communication Technology (IJ-ICT)
Vol. 12, No. 3, December 2023, pp. 236~241
ISSN: 2252-8776, DOI: 10.11591/ijict.v12i3.pp236-241

180 nm NMOS voltage-controlled oscillator for phase-locked loop applications

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Article Info

Article history:

Received Feb 2, 2023
Revised Apr 4, 2023
Accepted May 28, 2023

Keywords:

Phase-locked loop
Phase noise
Power consumption
Total harmonic distortion
Voltage-controlled oscillator

ABSTRACT

The voltage-controlled oscillator (VCO) is the primary device in the phase-locked loop (PLL) to produce the local oscillator frequency. The excessive phase noise of VCOs is the primary cause of PLL performance loss. This paper proposes the design and optimization of low phase noise and low power consumption for a 180 nm N-channel metal-oxide semiconductor NMOS VCO for PLL applications with P-channel metal-oxide semiconductor PMOS varactors and spiral inductors. At 2 V supply voltage, the optimized NMOS VCO has a power consumption of 21 mW, a phase noise of -130 dBc/Hz at 1 MHz offset and a total harmonic distortion (THD) of 3.9%. The proposed design is verified by PSpice simulations. A new criterion is proposed for optimizing NMOS LC oscillators.

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1. INTRODUCTION

The phase-locked loop (PLL) frequency synthesizers are one of the most important components of an integrated wireless transceiver system. PLLs are frequently used in wireless communication systems, digital signal processors, and microprocessors to synchronize the clock [1]. A Bluetooth transceiver's PLL must be able to supply frequencies from 2,400 to 2,480 MHz with channel spacing of 1 MHz. The performance of PLLs degrading mostly results from voltage-controlled oscillators (VCOs) excessive phase noise [2]. One of the most important components of every PLL is the VCO, which directly supplies the PLL's output signal [3]. VCOs provide the constant periodic signals needed for timing in digital circuits and frequency conversion in radio frequency circuits, which is a crucial and effective function for communication systems. The output frequency of the VCO depends on the control input, which is typically a voltage. An oscillator whose oscillation frequency is regulated by the input voltage is known as a VCO [4]. A VCO is in charge of producing a steady local oscillation (LO) signal. VCOs should typically have minimal phase noise, a wide frequency tuning range, and low power consumption [5]. Ring structures, relaxation circuits, or an LC resonant circuit can all be used to create CMOS VCOs.

Hadi *et al.* [6] provided an analysis of several delay cells for the ring oscillator, such as differential delay cells, starving current delay cells, and current follower cells. The findings indicated that compared to the other two types of delay cells, starved current delay cells consume less power and have a narrower frequency range. A VCO's performance is typically determined by its low phase noise, low voltage operation, low power consumption, high speed oscillation, small layout area, and wide tuning range. Among all VCOs, the LC-based VCO currently has the lowest level of phase noise. However, it has limits on the frequency

tuning range [2], [7]. A monolithic microwave integrated circuit (MMIC) VCO based on the balanced Colpitts with good phase noise and a wide tuning range is proposed in [8]. VCO based on the negative resistance, phase noise, output power consumption, and a large tuning range is presented in [9]. The proposed VCO produces a sinusoidal signal in the frequency range of 480 MHz-1.4 GHz.

Research by Chavan and Aradhya [10] presents a hybrid strategy for creating a VCO that can improve tuning range, oscillation frequency, voltage swing, and power consumption. The common-source active load-based inverter and the current-starved inverter were the two separate delay element types used in this design. A 175 GHz VCO is proposed in [11] based on a differential Colpitts oscillator to produce low-phase noise with a broad tuning range. To avoid unfavorable phase noise degradation, the VCO uses 41.9 mA of the 1.6 V supply voltage, resulting in a total of 67 mW of power. The primary challenge in designing integrated LC oscillators is low phase noise, low power consumption, and low output harmonic level, which is a measure of the VCO energy at harmonics of the oscillation frequency. These harmonics are generated by the non-linear self-limiting of active devices in the VCO circuit [12]. This paper presents on designing and optimization a low power, low phase noise, and low power consumption of 180 nm VCO with improved the total harmonic distortion (THD), which is suitable for PLL and Bluetooth applications. PSpice simulation tool and figure of merit (FoM) have been used for overall optimized design of integrated VCOs.

2. NMOS VOLTAGE-CONTROLLED OSCILLATOR CIRCUIT TOPOLOGY

A VCO is an electronic oscillator created to generate oscillation frequency using a regulated input voltage. By applying a controlled voltage, the oscillation's frequency may be changed. The number of components needed to create and maintain oscillation should be kept to a minimum when building a low-phase-noise oscillator. An oscillator using an LC tank, also known as an LC-VCO, is an excellent candidate to oscillate at a higher frequency with less phase noise and less power consumption in comparison to a ring oscillator. Figure 1 shows the NMOS cross-coupled VCO with current source and with two PMOS varactors. It is made up of the cross-coupled differential pair formed by M1 and M2. The positive feedback loop from the transistors M1 and M2 are used to generate negative impedance [13], [14].

$$R_{neg} = -2/g_m \tag{1}$$

where *gm* is the transconductance of the transistor.
The start-up condition of the oscillation states for the NMOS transconductance can be expressed as (2):

$$g_m > 2g_{eqv} \tag{2}$$

where g_{eqv} is the equivalent tank circuit conductance, $(g_{eqv} = g_L + g_v)$, g_L is the inductor conductance, and g_v is the varactor conductance. The conductance g_L and g_v are given as (3) and (4):

$$g_L = \frac{R_L}{(\omega L)^2} \tag{3}$$

$$g_v = \frac{\omega C_v}{Q_v} \tag{4}$$

The NMOS transistors M1 and M2 must be chosen for the same transconductance gm and considerable smaller than PMOS transistors. The PMOS transistors M3 and M4 represent the contrary connected varactors which controlled by a DC voltage supply. The transconductance is often designed to be roughly two times bigger than the needed amount in order to ensure that the VCO oscillation happens. Transconductance should be given, to determine the power consumption of the VCO which is calculated in (5) and (6):

$$P_{con} = 2I_D \times V_{DD} \tag{5}$$

$$I_D = \mu C_{ox} \frac{W}{2L} \left(V_{gs} - V_{th}\right)^2 = \frac{g_m^2}{2\mu C_{ox} \frac{W}{L}} \tag{6}$$

where *Vth* is the threshold voltage of the transistor and *Cox* is the oxide capacitance per unit area.

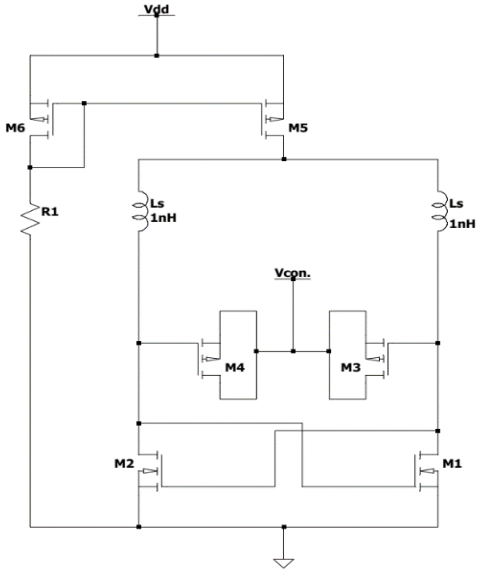

Figure 1. NMOS VCO circuit topology

3. PHASE NOISE OF VOLTAGE-CONTROLLED OSCILLATOR

The key difficulty in building integrated LC oscillators is keeping the power consumption low while reducing phase noise. Typical design strategies have tried to achieve low phase noise by using inductors with the most significant possible quality factor (Q) values. The phase noise of VCO in dBc/Hz at an offset frequency of Δω can be accurately estimated in (7) [15]–[17]:

$$L\{\Delta\omega\} = 10\log\left[\frac{\Gamma_{rms}^2}{2q_{max}^2} \times \frac{\sum \overline{i_n^2}/\Delta f}{\Delta\omega^2}\right] \quad (7)$$

Where Γ_{rms}^2 is the rms value of impulse sensitivity function and $\Gamma_{rms}^2 = 0.5$ for an ideal sinusoidal signal, q_{max} is the maximum charge swing, Δω is the offset frequency from carrier, and $\overline{i_n^2}/\Delta f$ is the sum of the current noise densities.

4. FREQUENCY TUNING

A tunable oscillator is essential for most wireless applications, meaning that its output frequency depends on a control input, often a voltage. The on-chip PMOS varactors are used to adjust the VCO's output frequency [18], [19]. The oscillation frequency is given as (8):

$$f_{osc} = \frac{1}{2\pi\sqrt{L_{tank}C_{tank}}} \quad (8)$$

where L_{tank} is the tank inductance and C_{tank} is the tank capacitance, which is the sum of the varactor`s capacitance and parasitic capacitance.

5. FIGURE OF MERIT

Due to the large range of design parameters, technologies, and design criteria used in oscillators, it is challenging to compare their performance. The majority of oscillator designers often provide a FoM number for their particular design. Typically, FoM is utilized to fairly evaluate the entirety of performances with comparable previously published works [14], [20]. Most researchers are focused on the FoM expression used to achieve low phase noise at high frequencies and minimal power consumption. However, it is not sensitive to harmonic distortion. In this paper the FoM expression to optimize low phase noise at high frequency, low power consumption, and low THD is given as (9):

$$FoM_{dB} = L\{\Delta\omega\} + 10\,log\left(\frac{P_c}{1mW}\right) + 20\,log(THD) \quad (9)$$

Where $L\{\Delta\omega\}$ is the single side band noise at an offset frequency $\Delta\omega$ in the $1/f^2$ region of the phase noise spectrum, P_C is the oscillator power consumption, and THD of the generated sinusoidal signal. Lower (more negative) *FoM* represents better VCO performance.

6. DESIGN AND OPTIMIZATION 180 NM NMOS VOLTAGE-CONTROLLED OSCILLATOR

The significant challenge in constructing integrated LC oscillators is reducing phase noise while keeping overall harmonic distortion and power consumption to a minimum. The drain current, transistor size, inductor, and varactor performance all affect the phase noise and power consumption. The selected variables for optimization of an integrated LC NMOS VCO are the inductor number of turns (n) and transistor channel width W_n. The optimization criterion has the form as (10) [21]:

$$\min FoM\ (W_n, n) \tag{10}$$

The proposed VCO has been designed and optimized for standard $L_n = 180\ nm$ CMOS technology with varying the transistor channel width W_n and inductor turns number n=2, 3, and 4. The VCO optimization criteria were verified and simulated using MATLAB and PSpice. The circuits have been simulated at a 2 V supply voltage and varied the control voltage from 0.5 to 2.5 V to observe the change in the frequency bandwidth. The optimization result is shown in Table 1. The optimization results depicted by the phase noise dBc/Hz, power consumption Pcon, THD, and FoMdB. From Table 1, the minimum value of FoMdB corresponds to the best optimization solution of the VCO.

Table 1. Optimization results of NMOS LC VCO

Inductor number of turns (n)	Transistor gate width W_n (nm)	Power consumption (mW)	Phase noise (dBc/Hz)	THD (%)	FoM (dB)
2	150	21.1	-130.45	3.97	-145.23
2	200	22.6	-130.82	5.51	-142.45
2	250	23.8	-131.11	5.65	-142.30
2	300	24.8	-131.33	8.20	-139.11
2	350	25.7	-131.52	7.95	-139.41
2	400	26.5	-131.68	10.84	-136.74
2	450	27.1	-131.80	11.41	-136.32
2	500	27.7	-131.91	13.42	-134.93
3	150	21.1	-131.94	6.59	-142.32
4	150	21.1	-132.35	7.68	-140.51

Figure 2 shows the effect of transistor channel width W_n in the FoMdB when the inductor number of turns is constant, n=2. The best measure performance when FoMdB$= -145.23\ dB$ at $W_n = 150\ nm$. The effect of W_n on phase noise when an inductor's number of turns is constant (n=2) is shown in Figure 3. However, Figure 4 represents the effect of FoMdB when W_n is constant and the inductor turns number n has varied. It can be noted that the minimum value of n represents the optimum performance for VCO.

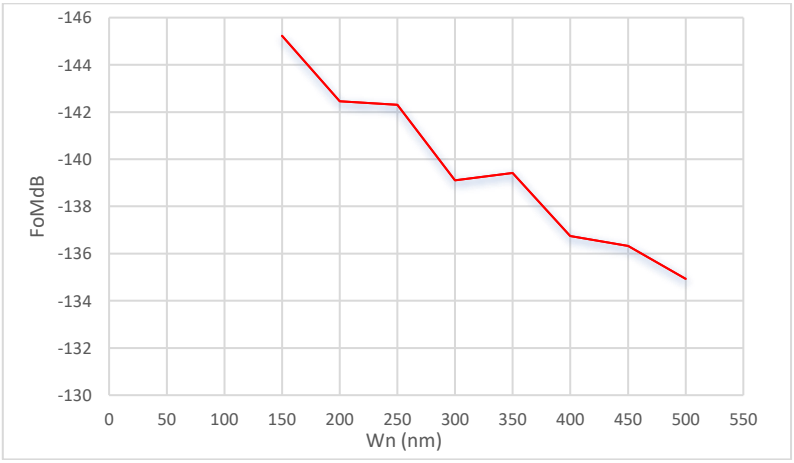

Figure 2. Effect of transistor channel width W_n in the FoMdB with inductor number of turns, n=2

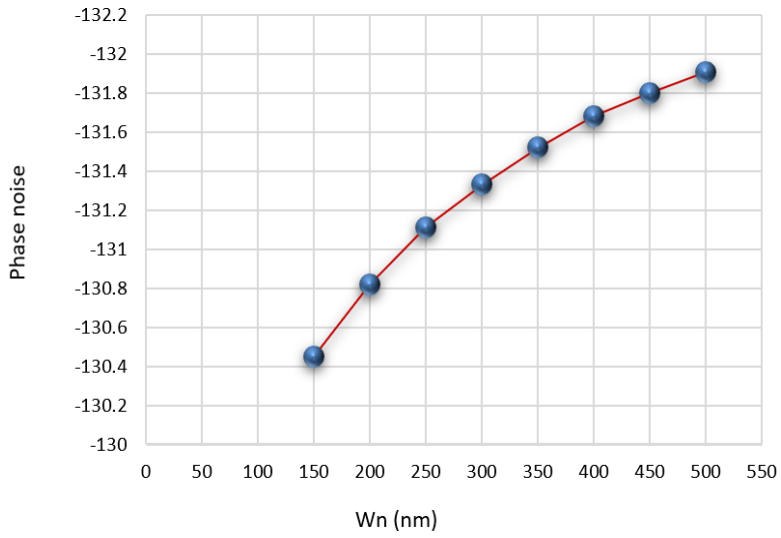

Figure 3. Effect of transistor channel width W_n in phase noise with inductor number of turns, n=2

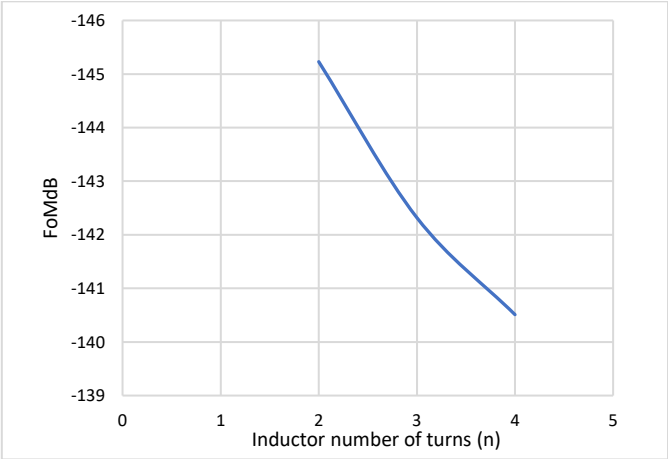

Figure 4. Effect of varying the inductor number of turns (n) in FoMdB with constant W_n

7. CONCLUSION

In this paper, optimization of the overall phase noise, power consumption, and THD for NMOS VCO in standard 180 nm CMOS technology has been presented. A wide range of frequencies has been obtained using MOS varactor technology when the voltage supply is varied from 0.6 to 2.5 V. The simulation results have measured a minimum FoMdB= $-145.23\ dB$, phase noise $L\{\Delta\omega\} = -130.45$ dBc/Hz @ 1 MHz offset frequency from 2.4 GHz carrier, Pcon=21.1 mW, and THD=3.97%. A tuning range of about 120 MHz was obtained using MOS varactors.

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