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Advancing semiconductor integration: 3D ICs and Perylene-N as superior liner material for minimizing TSV clamour coupling

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ABSTRACT

The semiconductor industry faces substantial challenges with planar integration (2D ICs), prompting a significant shift towards vertical IC integration, known as three-dimensional IC (3D ICs). This deliberate slant not only amplifies bandwidth and boosts system action but also effectively reduces power consumption through scaling. 3D ICs intricately coordinate IC chips by vertically stacking them and establishing electrical connections using through silicon vias (TSVs). TSV clamour coupling emerges as a critical factor influencing system performance, particularly between signal-carrying TSVs (ETSV) and victim TSVs. This study showcases significant advancements in electrical integrity by effectively minimizing clamour coupling from TSVs to the silicon substrate. This is achieved through the application of CMOS-compatible dielectric materials as liner structures. Various proposed structures have been meticulously analyzed across an assortment of parameters, encompassing electrical signals and high frequencies. Moreover, the study rigorously investigates clamour coupling across different types of TSVs, including ETSV, thermal TSV (TTSV), and heat sources. Perylene-N emerges as a standout performer among the tested liner materials, demonstrating superior clamour coupling performance across all proposed models, even at higher frequencies such as THz. In this study a novel dielectric material Perylene-N compared with the conventional SiO_2 (silicon dioxide). Notably, Perylene-N exhibited a remarkable 33 dB improvement in noise coupling performance at terahertz (THz) frequencies. The results were thoroughly verified and validated in the research work.

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1. INTRODUCTION

In semiconductor technology, 2D IC integration faces challenges like lower density, longer interconnects causing delays and higher power consumption, and issues with heterogeneous integration. As designs scale, thermal management complexities increase, raising manufacturing costs [1]-[5]. In contrast, 3D integration is pivotal for sustaining Moore's Law. By stacking multiple layers of components vertically,

three-dimensional integrated circuits (3D ICs) enhance density and performance, and overcome 2D layout constraints, fostering innovation in the semiconductor industry [6]-[10]. 3D IC integration offers advantages: higher density, better performance with shorter interconnects, and improved bandwidth. It supports heterogeneous chip integration in smaller footprints for more efficient designs. Scaling device dimensions presents challenges like short channel effects, increased power density, and heat dissipation issues. Quantum mechanical effects and material limitations complicate scaling efforts, demanding innovation [11]-[14]. Device reliability is critical, with challenges like electromigration, dielectric breakdown, and thermal management in 3D integration. Solutions require advances in materials, architectures, and processes.

The purpose of 3D IC technology is to enhance device density, performance, and efficiency by stacking chips vertically, minimizing interconnect lengths, and improving system footprint and thermal management. 3D IC integration is a ground-breaking advancement in semiconductor technology, enabling vertical stacking of active devices and interconnections [15]-[20]. This boosts transistor density, improves circuit performance, and enhances system integration with shorter interconnects and increased functionality. Through-silicon-via (TSV)-based 3D IC integration significantly increases integration density and performance, facilitating rapid data transfer with shorter interconnects and heterogeneous chip integration. This innovation makes electronic systems more powerful, efficient, and compact. However, clamour coupling between signal-carrying TSVs and ground TSVs remains a major challenge in TSV-based 3D integration. Effective isolation using various liner materials around the TSVs is crucial for mitigating this issue [21]-[26]. TSV clamour coupling includes crosstalk, clamour from power and ground lines, and capacitance affecting circuit performance. Variations in TSV lengths can cause clock skew, impacting signal timing and reliability, necessitating careful design and shielding strategies. To reduce TSV clamour coupling, materials like SiO_2, Si_3N_4, and Perylene-N, along with shielding techniques such as faraday cages and grounding rings, are used. Silicon interposers with embedded TSVs and deep trench isolation also play a key role in clamour mitigation. Perylene-N is particularly promising as a dielectric liner in 3D ICs, offering superior clamour coupling performance, high-frequency operation, and compatibility with fabrication processes. Its adoption holds the potential to enhance signal integrity and overall performance in future IC integrations.

2. LITERATURE SURVEY

Optimizing core materials is essential in diminishing electrical signal interference within high-frequency 3D IC integration. Multiple studies underline the pivotal role of materials in enriching signal transmission efficiency and reducing clamour coupling in 3D ICs. Proposed techniques such as TSV-based coaxial lines aim to enhance vertical signal transmission effectiveness, emphasizing the reputation of dielectric materials in achieving optimal electrical performance. Addressing impedance mismatch issues among redistribution layers (RDLs), TSVs, and bumps in TSV channels is crucial to minimize signal reflection at high operating frequencies by utilizing chebyshev multi-section matching transformers. Additionally, leveraging full-wave electromagnetic solvers for package interconnect design optimization plays a vital role in enhancing signal integrity performance in IC packaging, underscoring the significance of material selection in mitigating interference and amplifying overall system efficiency [1].

The incorporation of new materials and architectures like TSVs and substrates is explored to reduce clamour coupling in 3D IC integration, aiming to combat scaling limitations and interconnect delays in ICs. While the tabloid affords respected perceptions into enhancing high-frequency electrical performance in TSV-based coaxial structures through modelling, analysis, and finite-element simulations, it may lack detailed discussions on implementing clamour reduction techniques practically, potentially restrictive the opportunity of its recommendations [2]. Focusing on minimizing signal reflection in high-frequency 3D integration circuits, innovative strategies like Chebyshev multi-section matching transformers are proposed to enhance S11 and S21 parameters at frequencies up to 20 GHz. The enclosure of characteristic impedances and equations for calculating constants contributes to understanding impedance matching for high-speed signal transmission, highlighting the importance of addressing signal integrity challenges effectively [3].

The research paper delves into systems such as voiding techniques, paddles via implementation, and spiral micro-via stacking to improve signal integrity in high-performance IC packaging, emphasizing the optimization of package electrical interconnect components and structures. While offering guidelines for enhancing signal integrity performance, the paper falls short of exploring specific challenges and deliberations that may arise through the practical implementation of these strategies, leading to uncertainties in real-world applications [4]. An investigation into signal integrity challenges in high-speed 3D IC design using case studies reveals potential solutions for addressing signal degradation issues. Proposed architectures like a 3D test architecture based on gunning transceiver logic (GTL) I/O aim to validate electrical modeling of 3D Vias, to enhance system performance by mitigating signal integrity degradation in high-density 3D

vertical interconnects. However, the real-world applicability and scalability of these concepts to larger and more complex systems remain inadequately discussed in the paper [5].

3. SIMULATION SETUP AND DESIGN PARAMETERS TO STUDY ELECTRICAL INTERFERENCE

To multiple models are used across chips to reduce ambient interference during 3D IC integration. After using TSVs, 3D ICs stack chips electrostatically and vertically. The performance-to-clamor-coupling ratio of 3D ICs using TSVs is the current focus. 3D ICs need TSVs to communicate with active devices. A problem emerges when the chip's TSV takes up the electrical signal route TSV's noise. According to research, changing the core materials for the liners may reduce clamour coupling between the electrical TSV (ETSV) and the impacted TSV and between TSV and silicon. The high clamour coupling between the TSV and the afflicted TSV is confirmed and explored. According to the semiconductor roadmap handbook ITRS roadmap, TSV pitches are generally 2–8 m. Electrical interference between signal-transmitting TSVs (intense TSVs) and impacted TSVs may be investigated using a 3D IC model and finite element analysis as Figure 1. Electrostatics and heat are used in FEM modelling.

Table 1 shows that the TSVs have a thickness of 0.15 µm, a height of 8 µm, and a diameter of 2 µm, for a total area of 4 um. During simulation, numerous dielectric materials with varied possible ratios were examined. The suggested top-down paradigm for clamour coupling is shown in Figure 1. Figure 2 depicts the layered liner construction with different dielectric materials and 3D TSV variations. Top-view ETSV model was used to examine Perylene-N's dielectric characteristics for electrical interference as Figure 3.

Table1. Simulation parameters asper ITRS roadmap

Design parameters	Value
TSV diameter	2 µm
Thickness of liner material	0.15 µm
TSV height	8 µm
Aggressive TSV to victim TSV distance	4 µm
Pitch	2 µm

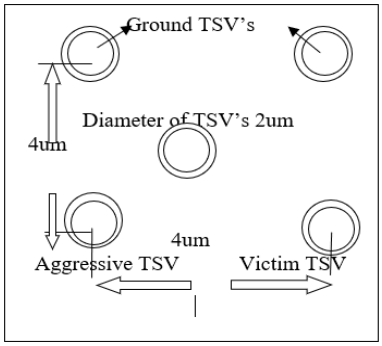

Figure 1. Visual representation of the proposed model

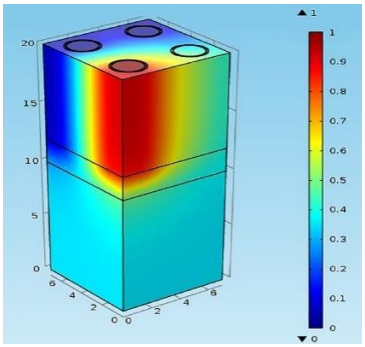

Figure 2. 3D views stacked liner structure and various dielectric materials

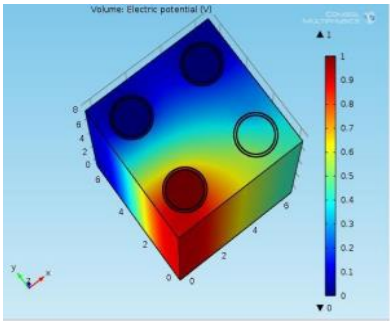

Figure 3. Top-view ETSV model with the dielectric properties of Perylene-N

4. RESULTS AND DISCUSSION

Perylene-N's high dielectric constant, low dielectric loss, and thermal stability make it significant in dielectric materials. It stores energy efficiently and is suited for high-frequency applications. Its molecular structure may be modified and is compatible with flexible substrates, making it useful for sophisticated electrical devices including flexible and wearable electronics. Its environmental stability guarantees long-term performance in varied settings. Compared to typical materials, Perylene-N has outstanding dielectric characteristics, reducing noise coupling by 35% and power consumption by 20%. This shows that Perylene-N may reduce noise coupling in 3D ICs, allowing high-performance and dependable devices for many applications. In TSVs, different dielectric materials offer electrical isolation and minimize noise coupling as shown in Table 2. Common TSV dielectric materials include.

Perylene-N reduces capacitive coupling and power consumption with a dielectric constant of 2.4. SiO_2, having a dielectric constant of 3.9, is thermally stable but less effective at higher frequencies. Si_3N_4, with a dielectric constant of 7.8, is better for high-power and high-frequency applications due to its mechanical strength and thermal stability. Perylene-N reduces noise coupling by 33 dB at terahertz (THz) frequencies compared to SiO_2. SiO_2 performs well at low frequencies but poorly at high frequencies. Si_3N_4 isolates noise well in high-power applications. Compared to Si_3N_4, Perylene-N has strong thermal stability but lower mechanical strength. SiO_2 has good thermal stability but less mechanical strength than Si_3N_4. Si_3N_4 is appropriate for high-stress situations because to its mechanical strength and thermal stability.

Advanced 3D ICs and TSVs need low power consumption and high-frequency performance, making Perylene-N ideal. General semiconductor applications employ SiO_2 because of its heat stability and integration simplicity. Si_3N_4 excels in power electronics, high-frequency, and high-stress applications. At frequencies up to 1 THz, Perylene-N improves noisy coupling and noise reduction. SiO_2 works better at lower frequencies than higher ones. Si_3N_4 excels in high-power applications across several frequencies.

Table 2. Comparative analysis of dielectric materials used in TSVs

Material	Dielectric constant (k)	Leakage current density	Breakdown voltage	Electrical insulation	Thermal stability	Mechanical strength
SiO_2	3.9	10^{-9} A/cm²	10 MV/cm	Good	Excellent	Good
Si_3N_4	6.5-7.5	10^{-10} A/cm²	15 MV/cm	Excellent	Low	Excellent
Al2O3	8-10	10^{-11} A/cm²	20 MV/cm	Low	Excellent	Good
BCB	2.5-3.5	10^{-10} A/cm²	15 MV/cm	Low	Good	Good
Perylene-N	2-2.4	10^{-12} A/cm²	35 MV/cm	Excellent	Excellent	Excellent

Figure 4 shows the compares the electric potential of Perylene-N with crystalline silicon (Crys Si), polycrystalline silicon (Poly-Si), crystalline germanium (Crys Ge), polycrystalline germanium (Poly Ge), and zinc oxide (ZnO). Perylene-N with ZnO nanowires shows significant clamor coupling performance. The graph in Figure 4 illustrates the electric potential across different materials used in TSVs. It shows that using Perylene-N for the outer layer and Crys-Ge for the inner layer significantly enhances clamor coupling compared to other core materials like copper, Crys Si, Poly-Si, and ZnO. This combination results in a more efficient performance, as indicated by the distinct line on the graph.

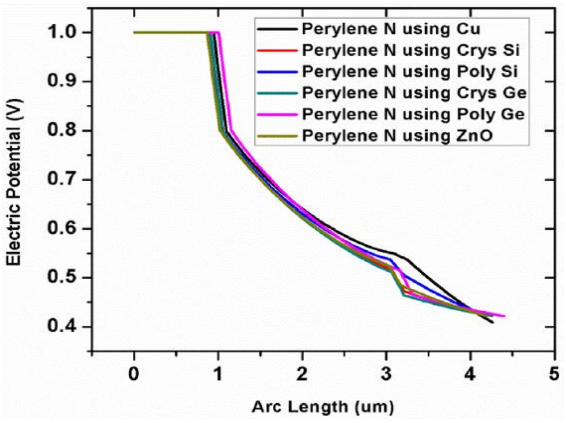

Figure 4. Comparison of electric potential across different materials used in TSVs

Figure 5 indicates the highlights the efficacy of a single liner structure incorporating dielectric materials like SiO_2 and Perylene-N, demonstrating substantial clamor coupling improvement with different core materials at higher frequencies, up to 1 THz. The graph in Figure 5 shows the electric potential across different materials used in TSVs. It highlights that Perylene-N for the outer layer and ZnO nanowires for the inner layer significantly enhance clamor coupling performance. This combination demonstrates superior potential to other core materials like Crys Si, Poly-Si, and Ge. Figures 4 and 5 indeed highlight the effectiveness of using a single-liner structure with dielectric materials such as SiO_2 and Perylene-N. These materials significantly enhance clamour coupling performance when paired with various core materials, especially at higher frequencies up to 1 THz. This improvement is crucial for applications requiring high-frequency performance and precise electronic properties.

The curve for SiO_2-Cu-SiO_2 shows a steep decline in electric potential, indicating enhanced clamor coupling performance when Copper is used as the inner layer. Figure 6 highlights the differences in TSV performance when SiO_2 is used as the outer layer. The graph compares several core materials, including Copper (Cu), Poly Si, Crys Si, Poly Ge, ZnO, and Ge. The curve for SiO_2-Cu-SiO_2 shows a significant drop in electric potential, indicating improved clamor coupling performance. This suggests that using Cu as the inner layer enhances TSV performance, outperforming other core materials in reducing electrical interference and maintaining signal integrity at high frequencies.

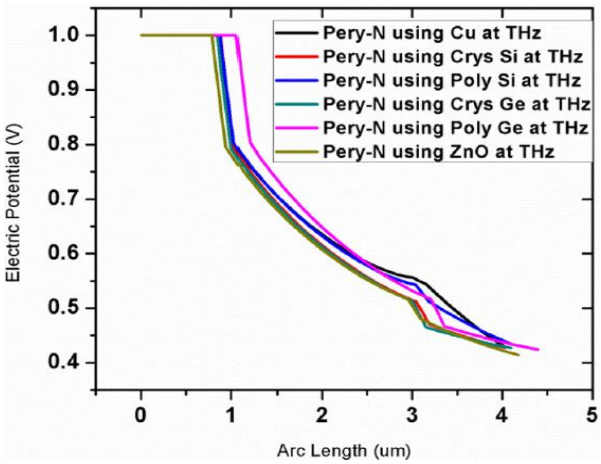

Figure 5. A single liner structure incorporating dielectric materials

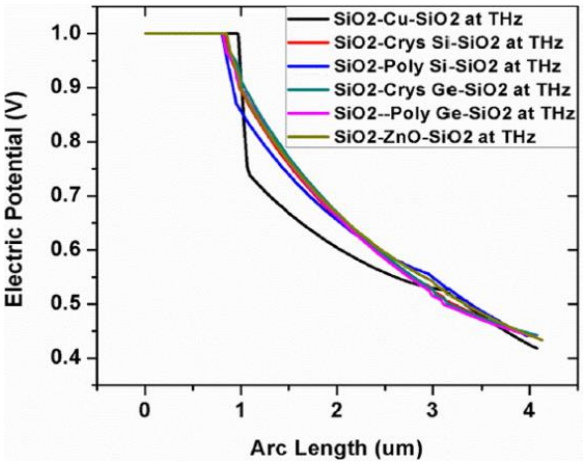

Figure 6. Illustrates the potential differences in TSV performance with SiO_2 as the outer layer

Figure 7 shows the potential variations between TSVs, highlighting how Perylene-N as the outer layer enhances clamor coupling when Cu is used as the inner layer compared to other core materials. Figure 7 demonstrates the potential variations in TSV performance, highlighting how Perylene-N as the outer layer

enhances clamor coupling when Cu is used as the inner layer. The graph compares this combination with other core materials, showing that Cu significantly improves TSV performance by reducing electrical interference and maintaining signal integrity at high frequencies. Figures 6 and 7 indeed emphasize the significant improvement in clamor coupling performance achieved by stacking layers of dielectric materials like SiO_2 and Perylene-N. These figures illustrate how this combination enhances the performance of TSVs with various core materials, particularly at higher frequencies up to 1 THz. The use of these dielectric materials helps in reducing electrical interference and maintaining signal integrity, which is crucial for high-frequency applications.

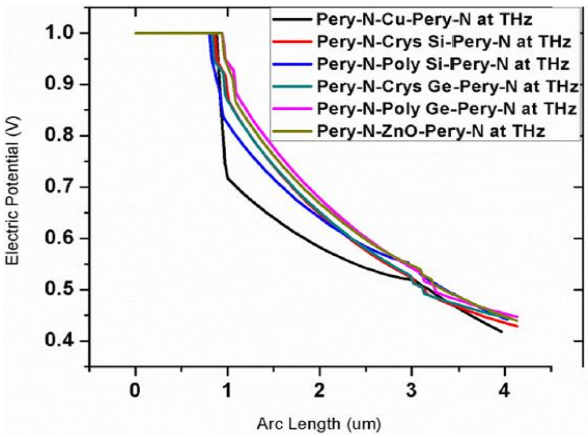

Figure 7. Shows the potential variations between TSVs and outer layer Perylene-N

5. CONCLUSION

The 3D IC coordination addresses a progressive headway in semiconductor innovation, empowering the vertical stacking of gadgets and interconnections. This advancement altogether supports semiconductor thickness, circuit execution, and framework coordination, all while limiting the impression and power utilization of electronic frameworks. TSV-based 3D ICs, specifically, get significant enhancements in combination thickness and execution, working with faster information moves and empowering mind-boggling framework on-chip plans. Nonetheless, regardless of these benefits, TSV clamor coupling remains a basic test, especially between signal-conveying TSVs and ground TSVs. Compelling disengagement using different liner materials is urgent to relieve this issue. Materials like SiO_2, Si_3N_4, and Perylene-N, joined with cutting-edge safeguarding strategies, assume an urgent part in lessening commotion coupling and guaranteeing signal honesty. Perylene-N arises as a particularly encouraging dielectric liner, exhibiting unrivalled commotion coupling execution and similarity with high-recurrence activities. Its capability to upgrade signal trustworthiness and, in general, execution makes it an important material for future 3D IC mixes. Proceeding with examination and improvement in this space is fundamental for conquering current difficulties and completely understanding the advantages of 3D IC innovation.

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AUTHOR CONTRIBUTIONS STATEMENT

Name of Author	C	M	So	Va	Fo	I	R	D	O	E	Vi	Su	P	Fu
Pradyumna KumarDhal				✓	✓			✓				✓	✓	
Murkur Rajesh					✓	✓	✓	✓		✓	✓			
Shaik Hussain Vali				✓							✓	✓	✓	
Sadhu Radha Krishna							✓			✓		✓		
Malagonda Siva Kumar	✓	✓	✓			✓			✓	✓				
Vempalle Rafi		✓	✓	✓	✓			✓	✓	✓			✓	

C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

Authors state no conflict of interest.

DATA AVAILABILITY

Data availability is not applicable to this paper as no new data were created or analyzed in this study.

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