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A comparative study and design investigation: scalable magnitude comparators across technology nodes

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ABSTRACT

In recent times, the convergence of innovative design technologies such as very large-scale integration (VLSI), cadence design systems, and field-programmable gate array (FPGA) has become crucial to address the growing demand for enhanced efficiency, scalability, and reduced power consumption in electronic designs. This paper introduces a novel approach to designing non-pipelined and pipelined scalable magnitude comparators (MCs), which integrates 4-bit MCs. The frontend implementation of the MCs is achieved using quartus prime, an FPGA board. The backend implementation is done using cadence design system, evaluated across the three distinct CMOS technology nodes. The literature review highlights the influence of technology scaling on area, power consumption, and propagation delay, analyzing various comparator designs and their associated trade-offs. The results provide valuable insights into the design and optimization of MCs for future applications in image processing and nano computing.

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1. INTRODUCTION

The selection of an arithmetic system plays a crucial role in shaping the design of a digital system. It influences factors such as the number of required operations, the signal activity level, and the operator strength or complexity. Design of integrated circuits (ICs) is realized architecture level [1], [2], device level, and circuit level abstractions [3], [4]. The primary function of a magnitude comparator (MC) is to compare two binary numbers, starting with the least significant bit. A 4-bit MC specifically handles the comparison of 4-bit binary values, yielding results such as greater than (A > B), less than (A < B), and equal to (A = B). The number of bits compared is influenced by factors like area, static power, and dynamic power consumption. Various technology nodes are available for implementation, each suited to different scenarios. As technology advances, the size of the components typically decreases. MC plays a crucial role in arithmetic units within microprocessors, controllers, and various digital design systems. One of its primary applications is in decoding within computer systems, as well as in control logic and error detection during data transmission [5]. It has a significant application impact in image and signal processing applications [6], [7], analog-to-digital converters [8], [9], and IoT applications [10], [11]. Various implementations of MC logic,

such as CMOS [12], transmission gate, pass transistor [13], gate-diffused input (GDI) approaches [14]-[17], and carbon nano tube FET [18] have been explored. While the GDI approach excels in minimizing propagation delay, transistor count, and power consumption, it struggles with achieving a full rail-to-rail swing. The reduced swing voltage results in slower switching, which can hinder device performance. Addressing this slow switching issue is essential to prevent a decrease in operational speed.

The area, along with static and dynamic power, significantly affects the number of bits that can be compared. As the number of bits increases, issues such as area constraints, power consumption, and propagation delay become more pronounced. It is important to note that leakage power increases proportionally with the device's size, which can decrease overall efficiency. Therefore, choosing the smallest possible size is generally recommended. A key advantage of this approach is that as feature size decreases, the channel length shortens. While this helps lower the threshold voltage, it can also lead to an increase in sub-threshold leakage current. The exploration of implementing MCs over technology nodes is thus significant [19]-[22]. Alternatively, in literature, comparators have been realized using quantum cell automata technology [23]-[25], XOR and OR gates [26], and majority logic [27]. Figure 1 illustrates the block diagram of a 4-bit MC, this paper's fundamental unit of consideration.

In this research paper, scalable MC's of 4, 8, 16, 32, and 64 bits are designed and implemented on a field-programmable gate array (FPGA). Additionally, at the physical design level, comparators are analyzed using 180 nm, 90 nm, and 45 nm CMOS technology. The paper presents a detailed comparison of area and power consumption results. Figure 2 depicts a 64-bit two stage pipelined MC.

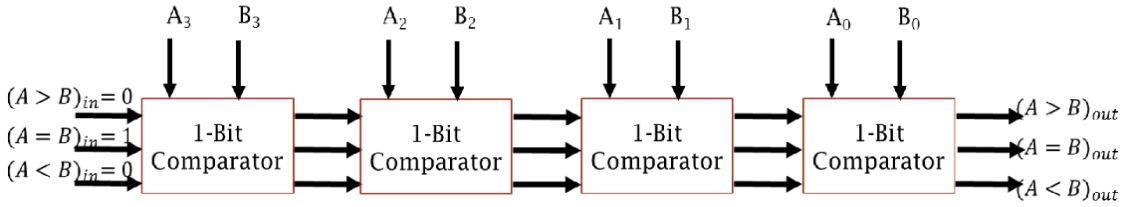

Figure 1. Representation of 4-bit MC

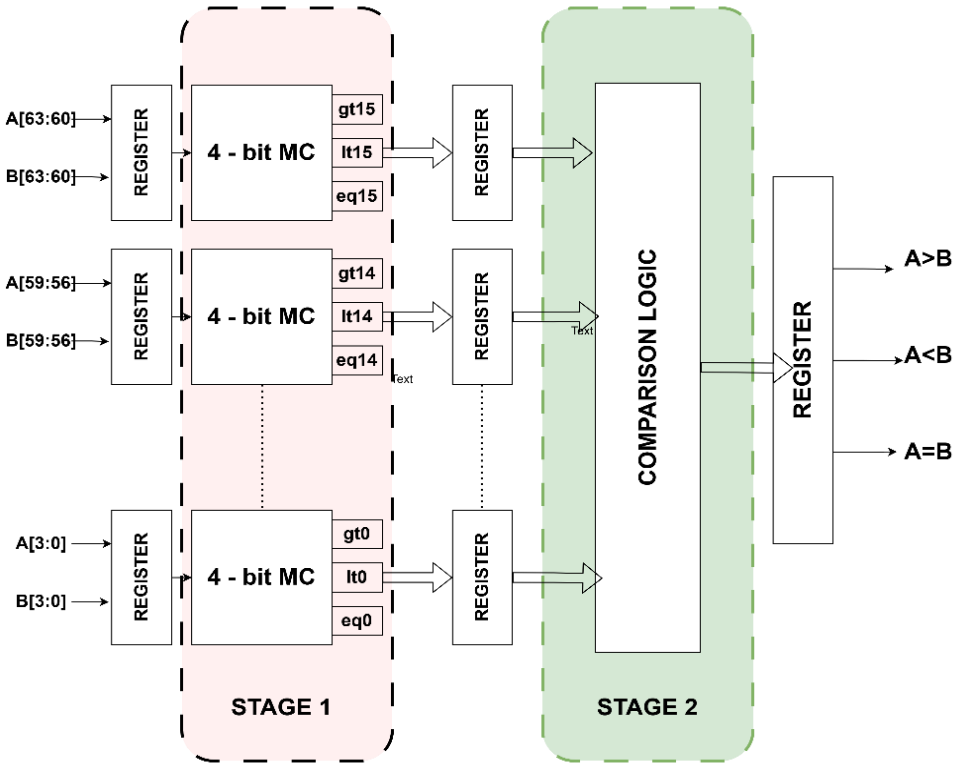

Figure 2. Two stage pipelined architecture of 64-bit MC

It also provides an overview of the comparator design process in Quartus and its implementation on FPGA. Performance metrics such as total power consumption, switching power, leakage power, sequential logic power, combinational logic power, and total area utilization are evaluated for each CMOS technology node. The paper is structured as follows: section 2 presents the design methodology and section 3 discusses the results. The final section provides the conclusion.

2. RESEARCH METHOD

The design flow for the scalable MC starts with FPGA design using Intel Quartus software. In this phase, a Verilog description and testbench are developed, followed by compilation, pin configuration mapping, and testing on the FPGA, Altera DE1-SoC board-Cyclone V- 5CSEMA5F31C6, to validate the output. Once the functionality is confirmed, the process transitions to the physical design phase. During this phase, the register-transfer level (RTL) viewer and waveform are generated using Cadence Nclaunch, providing insights into the design's behavior. The design is then synthesized using Genus, with an remote command (RC) script guiding the synthesis process. Cadence software is a suite of electronic design automation (EDA) tools widely used in the semiconductor industry. It supports the design and verification of ICs and PCBs. The software covers various design aspects, mainly including schematic capture, simulation, synthesis, layout, and verification. Cadence is particularly known for its applications in very large scale integration (VLSI) design and custom IC design, offering a comprehensive solution for the development of complex electronic systems.

In the semiconductor industry, a graphic data system (GDS) file is a binary format that is necessary for exchanging and storing IC layout information. Standardizing geometric and layer data, it makes EDA tools more well-matched with one another and promotes collaborative design. In order to create photomasks for the semiconductor manufacturing process, GDS files are essential since they specify the complex patterns needed for the fabrication process.

The paper highlights the below objectives:

- Design scalable non-pipelined and pipelined MC circuits in Quartus.
- RTL simulation for MCs.
- Generate physical layout using Cadence.
- Create GDS file for 180 nm, 90 nm, 45 nm technology.
- Comparison of power, delay and area across technology.

The physical design phase progresses with the use of Cadence Innovus, where key steps such as netlisting, floorplanning, power planning, standard cell placement, and routing with timing optimization are carried out. Clock tree synthesis is performed to ensure efficient and reliable distribution of the clock signal. Figure 3 illustrates the physical design of 64 bit non-pipelined comparator, synthesized at 90 nm CMOS technology.

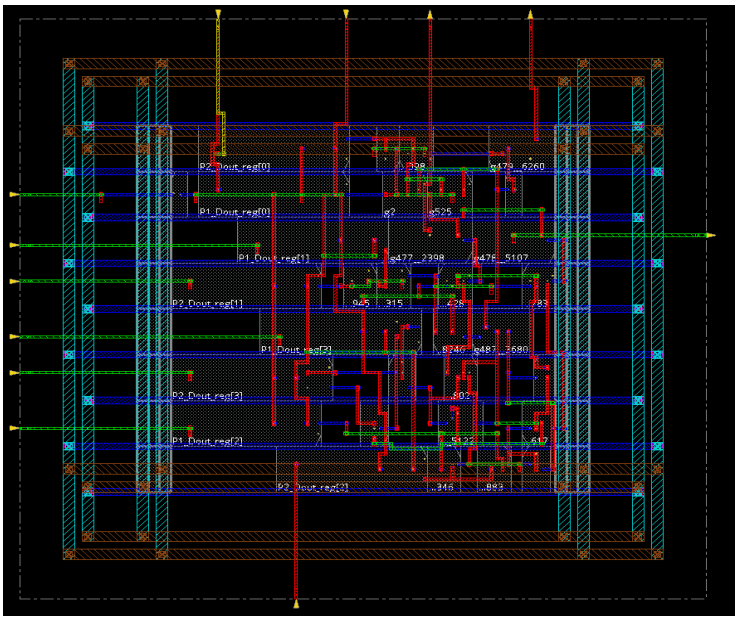

Figure 3. Physical design of 64-Bit non-pipelined MC at 90 nm

After completing these processes, further optimization is carried out using engineering change order (ECO) techniques and NanoRoute. This stage is essential for improving the overall efficiency and performance of the design. Verification steps, including design rule check (DRC) and connectivity checks, are also performed to ensure the design's accuracy and integrity. As the design nears completion, design files, netlists, and the GDS file are generated. Optionally, a 3D model of the design can also be created. The final steps involve rigorous verification to ensure that the design complies with DRC and connectivity rules while meeting all specified requirements and design objectives. This systematic design flow ensures a smooth progression from conceptualization to the finalized and fully verified scalable MCs.

3. RESULTS AND DISCUSSION

The non-pipelined and pipelined versions of the 4-bit, 8-bit, 16-bit, 32-bit and 64-bit MCs were targeted on Altera DE1-SoC board-Cyclone V- 5CSEMA5F31C6. The designs were tested for a random set of 5000 test vectors. The functional simulation result is depicted in Figure 4. The outputs gt, ls, and eq specifies the greater than, less than and equal to conditions with respect to the magnitudes of inputs a and b.

The synopsys design constraint (SDC) files were set and value change dump (VCD) files were generated to determine the power and maximum frequency of operation. Comparison of the results of power and maximum frequency of operation of the magnitude compartor for varied widths are summarized in Table 1. A comparison of the power delay product (PDP) is presented in Figure 5.

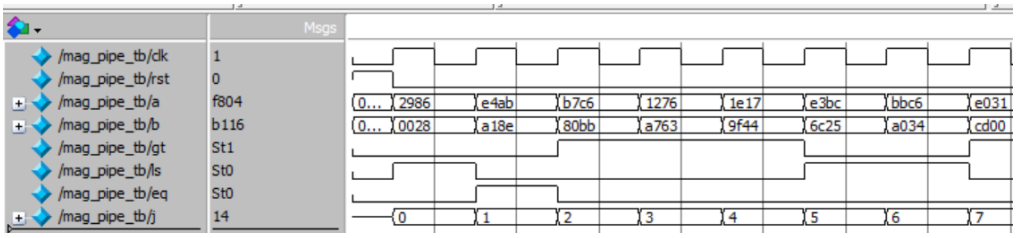

Figure 4. Simulation result of a 64-bit pipelined MC

Table 1. Power and maximum delay comparison of comparators of varied widths - Altera DE1-SoC board

Comparator	Power (mW)	Delay (ns)	PDP (pico Ws)
4 bit - Non Pipelined	1.46	1.9	2.774
8 bit - Non Pipelined	4.29	2.2	9.438
16 bit - Non Pipelined	26.02	2.7	70.254
32 bit - Non Pipelined	45.23	3.5	158.305
64 bit - Non Pipelined	65.12	5.1	332.112
4 bit - Pipelined	1.1	1.8	1.98
8 bit - Pipelined	3.2	1.8	5.76
16 bit - Pipelined	6.6	1.8	11.88
32 bit - Pipelined	12	1.9	22.8
64 bit - Pipelined	17	1.9	32.3

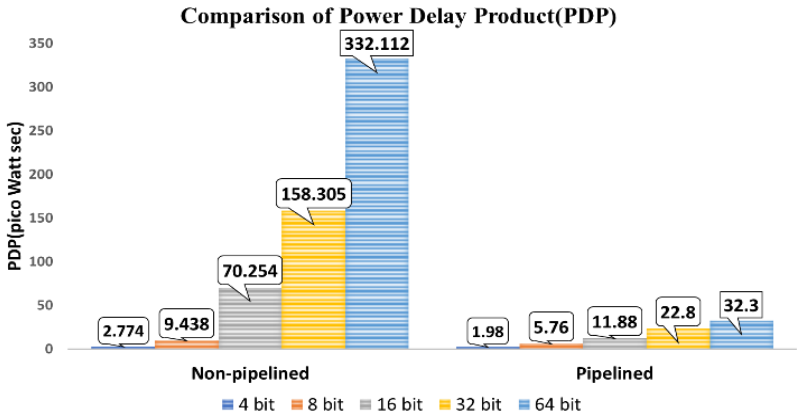

Figure 5. PDP metrics of comparator designs - Altera DE1 SoC board

The power of MC's implemented on FPGA shows low power consumption by pipelined architectures when compared with the non-pipelined architectures. Pipelined architectures speed up the operation. On the whole, the results depict the reduction in PDP of the 4-bit, 8-bit, 16-bit, 32-bit, and 64-bit pipelined multipliers by 29%, 38%,83%, 85%, and 90% respectively. It is evident that as the the number of bits of comparator scales up, the pipelined architecture is preferred compared to the non-pipelined architectures. Additionally, the designs were synthesized using Cadence genus tool with the CMOS technology libraries – 180 nm, 90 nm, and 45 nm. The power, delay, area and PDP of the designs generated for the various technology nodes for the pipelined and non-pipelined architectures are summarized in Table 2. A comparison of the PDP of the comparator designs across various technology nodes is depicted in Figure 6.

Table 2. Power, delay and area comparison of comparators of varied widths across various technology nodes – Cadence

Bits	Technology node	Non-pipelined					Pipelined				
		Power (mW)			Delay (ns)	Area (μm^2)	Power (mW)			Delay (ns)	Area (μm^2)
		Static	Switching	Total			Static	Switching	Total		
4 bit	180 nm	0.54	0.21	0.75	0.797	1034	0.42	0.23	0.65	0.387	2036
	90 nm	0.15	0.06	0.21	0.564	308.8	0.04	0.14	0.18	0.321	421.1
	45 nm	0.1	0.07	0.17	0.355	252	0.02	0.11	0.13	0.215	311
8 bit	180 nm	0.94	0.3	1.24	1.424	1879	1.11	0.24	1.35	0.646	2228.6
	90 nm	0.26	0.07	0.33	0.933	566	0.30	0.05	0.35	0.384	677.4
	45 nm	0.18	0.09	0.27	0.501	421	0.2	0.04	0.24	0.388	511
16 bit	180 nm	1.84	0.47	2.31	1.704	3918	2.09	0.4	2.49	0.646	4134.7
	90 nm	0.48	0.1	0.58	1.645	1067	0.56	0.08	0.64	0.384	1251.9
	45 nm	0.32	0.13	0.45	0.849	654	0.36	0.06	0.42	0.402	876
32 bit	180 nm	3.36	0.82	4.18	1.683	7274	4.02	0.74	4.76	0.646	7920.1
	90 nm	0.87	0.14	1.01	1.7	2165	1.07	0.14	1.21	0.384	2388
	45 nm	0.6	0.19	0.79	1.586	1232	0.71	0.09	0.80	0.402	2132
64 bit	180 nm	6.91	1.58	8.49	1.619	14968	7.88	1.42	9.30	0.646	15474.3
	90 nm	1.75	0.29	2.04	1.711	4429	2.08	0.29	2.37	0.384	4650.3
	45 nm	1.24	0.34	1.58	1.667	3954	1.37	0.17	1.54	0.375	4783

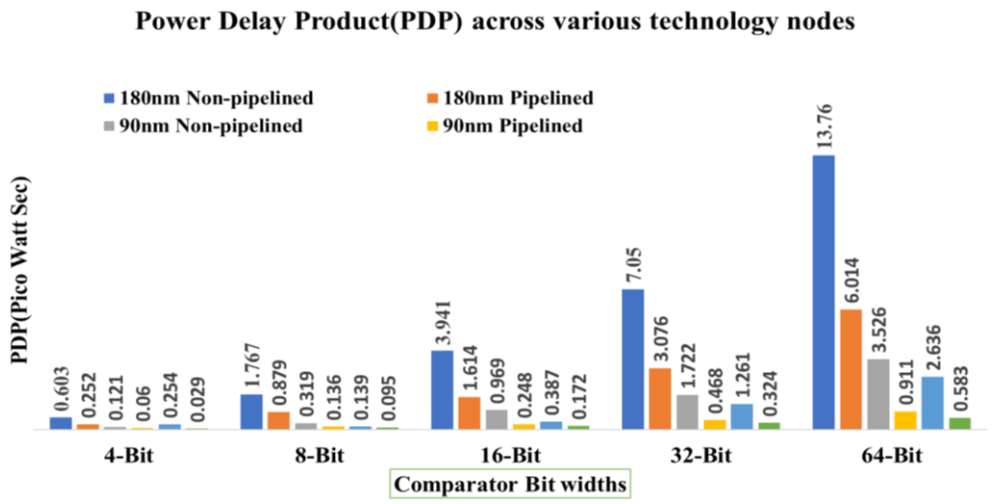

Figure 6. PDP metrics of comparator designs across technology nodes – 180 nm, 90 nm, 45 nm

In the case of 180 nm technology, switching power consumption is the primary contributor to overall power use, while for 45 nm technology, internal power consumption is the most significant factor. All three technologies demonstrate very low leakage power consumption. Additionally, both the 180 nm and 90 nm technologies show higher sequential logic power consumption compared to the 45 nm technology. This is primarily because sequential logic circuits typically utilize more transistors than combinational logic circuits.The PDP of all 4, 8, 16, 32, and 64 bit comparators present a 95% reduction in PDP as they transit from 180 nm to 45 nm from non-pipelined architecture to pipelined architectures.

The 45 nm process technology exhibits higher combinational logic power consumption compared to the 180 nm and 90 nm technologies. This is because combinational logic circuits generally incorporate more complex gates than sequential logic circuits. Overall, the 45 nm manufacturing technology offers the best performance-to-power ratio. One significant finding is the total area metric, which indicates the physical space occupied by each process technology's design. As process technology advances, there is a clear trend of decreasing area, evidenced by an average reduction of 75% for 4, 8, 16, 32, and 64 bit comparators for transition from 180 nm to 45 nm technology. This decrease is attributed to the use of smaller transistors, which enables greater functionality to be integrated into a more compact space. The key takeaway is that, as demonstrated by the 45 nm example, a lower process technology results in a significantly smaller area. This is a crucial advantage in modern chip design, allowing for increased functionality or higher density within the same physical constraints. Importantly, the core design integrity is maintained despite these advancements, focusing on optimization rather than a complete overhaul of the underlying principles.

4. CONCLUSION

This paper explores the design of a scalable MC - 4, 8, 16, 32, and 64-bit non-pipelined and pipelined utilizing Quartus Prime, FPGA technology, and the cadence design system across three technology nodes: 180 nm, 90 nm, and 45 nm. The results include 3D layouts and GDS files for each technology node, demonstrating that the 45 nm process technology has the lowest overall power usage. The power consumption analysis highlights several factors, including internal power, switching power, leakage power, sequential logic power, and combinational logic power, with the 45 nm technology showing a superior performance-to-power ratio. The area comparison reveals a significant reduction in physical size as technology nodes advance, while the instance count remains consistent, reflecting stable underlying design logic across all nodes. In summary, this study offers valuable insights into the trade-offs between power consumption, performance, and physical size in the design of a 4-bit MC across different technology nodes.

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Umamaheswari Ramalingam	✓	✓		✓		✓	✓	✓	✓	✓	✓	✓	✓	
Ashlin Leon A. S.			✓	✓				✓			✓			
Sinthia Panneer Selvam			✓	✓			✓			✓	✓			
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Arunkumar Kuppusamy			✓		✓	✓						✓		

C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

Authors state no conflict of interest

DATA AVAILABILITY

Data availability is not applicable to this paper as no new data were created or analyzed in this study

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