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Optimized ultra-low power and reduced delay GNR Ternary SRAM using a 7-transistor architecture

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ABSTRACT

Greater need and evolution in electronics require a memory device that can go with a decreased power delay, SRAM plays an important role as a storage element in digital circuit design. Power and delay are vital problems faced by today's RAM technology. It is necessary to lessen the power and increase the speed. There is a need to reduce power utilization and time delay. The proposed method is seen in the Electronics technical tool H-Spice technology. The technique proposed on DRG 7T- transistors SRAM consumes less power and delay. After the analysis and enhancement of the circuit, this approach gives the power delay product of the graphene nanoribbon (GNR) 7T SRAM as 80% at 0.7 V, 59% at 0.8 V, 34 % at 0.9 V, which is much less when compared to conventional SRAM power delay product.

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1. INTRODUCTION

Static random-access memory (SRAM) is the fundamental storage element and as quick storage capacity. SRAM is one bit storage unit. Itis utilized as latch to store one bit data. It is the memory element free from regular refreshing to reduce the complexity. In SRAM it is easy to acquire the data. SRAM data depends on the power availability provided to it. It can hold on the data until power is available. As of its high performance it is abundantcost. 6Transistors SRAM and 5Transistors SRAM is simulated on Tanner EDA tool. It is found the occupied area and utilization power is decreased for the 5Transistor SRAM. 6Transistor SRAM occupies additional area and extra power but 5Transistor as the problem while performing write '1' operation [1]. SRAM with less utilization power and less time delay is found by the refitting done in cell in order to make it as sense amplifier to decrease PDP [2]. Column structure different 5Transistor cell decreases the power and increases speed then 6Transistor [3]. 8Transistor SRAM through 1Write1Read gives less delay and decrease in power than 6T SRAM. 8T SRAM through additional circuit of RS FlipFlop is utilized to preserve the content [4]. By tanner tool differentiation among 6T, 5T, and 4T found to be that 4T SRAM presents better results in calculations of power capacity and speed in 22 nm technology [5]. 8Transistors 4bit SRAM power utilization is lower as the given voltage capacity goes down at distinct supply voltages [6]. By using predictive technology model analysis is taken for 6T SRAM for power utilization with stability, channel length, and delay [7]. 6Transistors SRAM is executed and symbol is done for it. By working on cadence, simulation SRAM array is designed and executed [8]. 5T SRAM is formulated for less delay applications [9]. By using suitable leakage current methods leakage currents and supply voltage can be minimized. 7T SRAM is formulated in cadence tool under 45 nm technology to observe the leakage currents

effect [10]. To evaluate the resilience of a stability analysis of an SRAM circuit based on graphene nanoribbon field-effect transistors (GNRFETs) under process variation is observed. Mohammed and Chowdhury [11] five-line coupled ML GNR interconnects and actively shielded five-line MLGNR are simulated at 10 nm and 7 nm at 0.8 V applied voltage and found that crosstalk noise in ML GNR is smaller [12]. Efficient charge recovery logic (ECRL) based inverter and positive feedback adiabatic logic (PFAL) based inverter are presented. ECRL 8-bit ALU performing 4 arithmetic and logic operations [13]. On/off current, field effect mobility, band gap electrical properties are dependent on the GNR width. Fabrication of the SI NWs with different diameters is seen [14]. GNR heterojunction electronic structure and charge transport is given. Fabrication electronic properties of grapheme nano ribbon are seen [15]. Plotting a valuable 6T-SRAM cell with shorted Gate mode FinFET transistors [16]. The GNRFET-based three-valued logic simulation with HSPICE 32 nm technology tool is used in D-Latch to decrease power and latency [17]. This work observed that many SRAMs were implemented to get less power and delay. Still, this suitable implementation for ternary logic in the GNR fabrication method is a new proposed method to get good with much less power and delay [18]. The proposed paper described as follows: section 2 implementation of 6T SRAM, section 3 implementation of DRG SRAM, section 4 results, and section 5 conclusion.

2. IMPLEMENTATION OF CMOS 6T SRAM

Conventional 6T SRAM as shown in Figure 1 as six transistors 2 PMOS and 4 NMOS transistors. Two inverters are connected back-to-back NMOS transistors are the transistors utilized for read and to write in the data in the cell [19]. The two-bit lines BL and BLB are utilized for pre charging and dropping the charge present in memory unit. The WL is connected to both gates of the NMOS transistors. WL line is used for activating the two access NMOS transistors while performing reading and writing the data. The interconnected inverters are given with supply voltage V_{DD} and ground V_{SS}. One inverter's output is used as another's input. inverter vice versa. The output of two inverters is given as Q and QB.

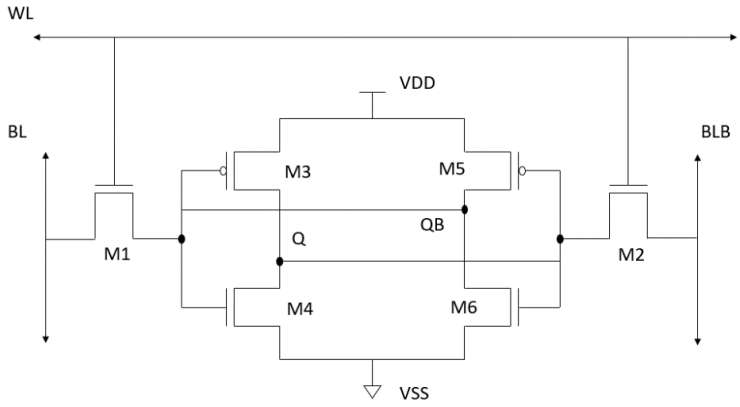

Figure 1. Conventional 6T SRAM circuit diagram

2.1. Read operation

- For logic 1 operation bit-lines are pre charged to VDD.
- M1 and M2 access transistors gets ON when read volt is applied to the gates.
- M2 starts discharging through BLB and M2 will go in saturation region then voltage decreases.
- M1 remains same because of no current flow and voltage remains at logic 1.
- For logic 0 operation bit-lines are pre charged to VDD.
- M1 and M2 access transistors gets ON when read is applied to the gates.
- M1 starts discharging through BL and M1 enters into saturation region and voltage decreases.
- M2 remains the same because of no current flow and voltage remains at logic 1.

WRITE OPERATION

- To write the data bit lines should be forced to logic 0.
- Write logic is applied to gates of M1 and M2 access transistors. M1 and M2 transistors gets ON.
- M2 discharges and M4 transistors turns off and data is written at the output.

Figures 2-4 shows the Waveforms in conventional 6T SRAM at 0.7 V, 0.8 V, and 0.9 V in 32 nm technology. Table 1 shows 6T SRAM power and delay values at distinct voltages in 32 nm technology, this SRAM is considered as the conventional SRAM in the implementation of many circuits, same has been simulated at different voltages simulated outputs Waveforms for different voltages plotted in Figures 2-4. Figures 2-4 shows the Waveforms in conventional 6T SRAM at 0.7 V in 32 nm technology. Table 1 shows 6T SRAM power and delay values at distinct voltages in 32 nm technology.

Table 1. Simulated results of the conventional 6T SRAM in 32 nm technology

Design analysis	Voltage (V)	Power (µW)	Delay (ns)
SRAM-32 nm	0.7	49.45	2.64
SRAM-32 nm	0.8	120.32	2.64
SRAM-32 nm	0.9	211.04	2.63

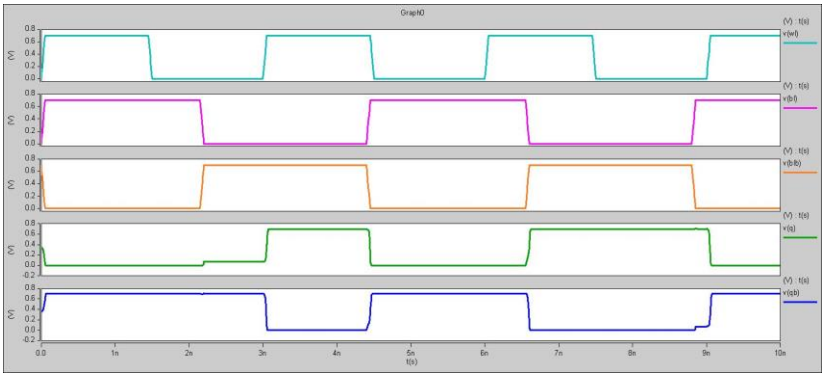

Figure 2. Waveform of 6-Transistor SRAM at 0.7 V

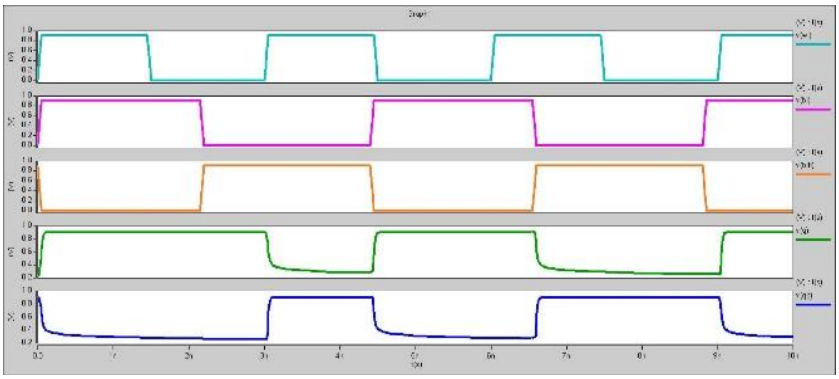

Figure 3. Waveform of 8-Transistor SRAM at 0.8 V

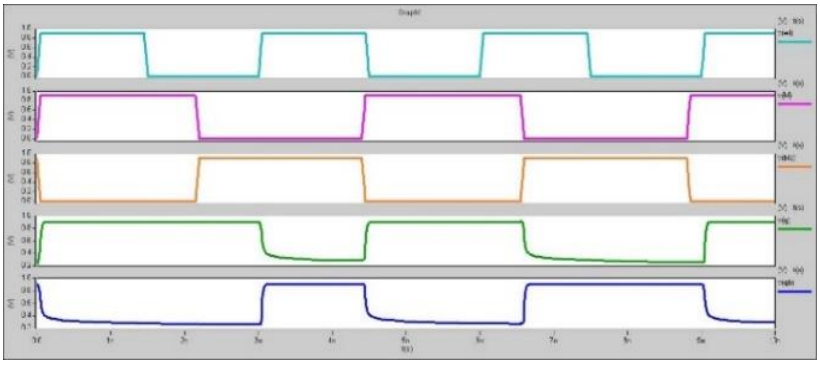

Figure 4. Waveform of 9-Transistor SRAM 0.9 V

2.2. Graphene nano ribbon properties

Single layer graphene is a blend of numerous hexagons. By noticing Figure 5 the manner in which we are estimating the width and length of the graphene nano ribbon can be noticed flat line addresses the length of the graphene nano strip and its unit of the estimation is nano meter [20], [21]. The upward line is the width of the graphene nano strip. Its unit of the estimation is nano meter.

There are two sorts of graphene nano strips. One is zigzag and other is arm chair graphene nano ribbon. In light of the sort of the edges in the graphene nano ribbon it is named as armchair and zigzag [22]. Zigzag course of action of the GNR is displayed in Figure 6. Zigzag is graphene nano strip with a few hexagons interconnected. Zigzag graphene nano strips (ZGNRs) are consistently metallic [23]. Due to the metallic nature it is seldom utilized.

The other sort of the graphene nano strip is armchair type GNR lace. Figure 7 is the arm chair structure graphene nano ribbon course of action by noticing the edges [24]. Armchair type graphene nano lace is same as zigzag with 120 degrees pivot of the zigzag. Armchair type graphene nano lace is semiconductor or metallic.

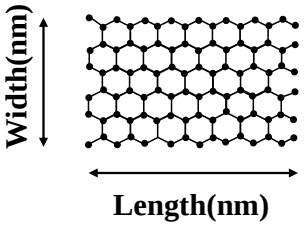

Figure 5. Length and width parameter measurement

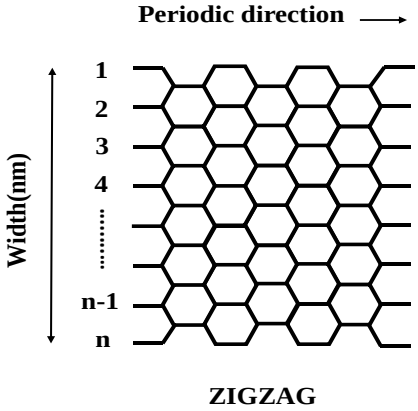

Figure 6. Zigzag structure of the graphene nano ribbon [5]

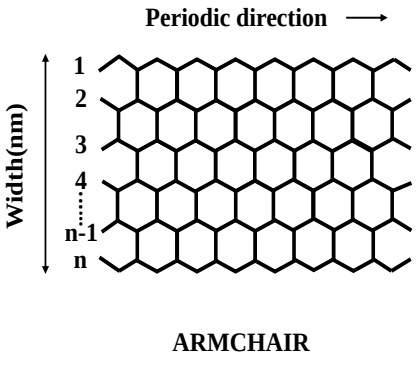

Figure 7. Armchair structure of graphene nano ribbon

By observing Table 2 it can be observed the behavior of the GNRFET depending on the dimer lines (N), for small bandgap conductivity is more and for highest band gap conductivity is less. By using the below mathematical equation width of the GNR can be calculated depending the dimer lines and carbon distance.

$$W_d=\sqrt{3}a(N+1)/2 \quad (1)$$

a=0.142 nm is the carbon-to-carbon bond distance
N is number of Dimmer lines
W_d is the width of the GNR

Table 2. Dependence of GNRFET behavior on dimer lines (N)

Dimer lines, N	Band gap	Ion/Ioff	Order of Ion/Ioff	Ion
8, 11, 14, 17	Small	lowest	~10^1	Highest
6, 9, 12, 15, 18	Moderate	high	~10^6	High
7, 10, 13, 16	highest	highest	~10^6	low

Figure 8 shows how the value of carbon-to-carbon distance i.e., a is taken can be observed by seeing the figure. It is the element used in calculating the width of the graphene nano ribbon [25]. The threshold voltage of the gnr can be calculated by using:

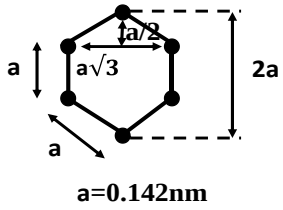

Figure 8. structure for the carbon-to-carbon distance

$$Vt=bg/3e$$

b_g is the band gap,
e is the unit electron charge, 1.6×10^{-19} C

$$bg=2|\delta|\Delta E$$

δ is the interlayer distance,
ΔE is the energy gap between sub bands,

$$\Delta E=\pi hVf/Wd$$

v_f is the fermi velocity,
h is the plank's constant with value of $6.5821x10^{-16}$ eVs,
W_d is the width of the GNR

2.3. Ternary logic

Binary logic is a two values logic with either 0 or 1. Binary logic as base 2. Multi valued logic is a logic with three or more logics. As shown in Table 3 Ternary logic is also a multi valued logic. Ternary logic as base 3. Ternary logic as 0, 1, and 2. The voltage values of the ternary logics are 0 V, 0.45 V, and 0.9 V. For 0 V applied voltage logic is 0. For 0.45 V applied voltage logic is 1. For 0.9 V applied voltage logic 2.

Table 3. Ternary logic values

Voltage value	Logic value
0 V	0
0.45 V	1
0.9 V	2

2.4. GNRFET ternary half adder

The proposed half adder is constructed as fallows. From Figure 9 here we have taken A and B are the input decoders through which we are sending A0, A1, A2 variables from the input decoder A and similarly with the input decoder B the variables are B0, B1, B2. For the Sum operation, here we implemented with 6- AND gates and 2- OR gate, in the first step the inputs which are coming from the Decoders are firstly given to the 3-Logic AND combinations, the inputs are (A2, B0), (A1, B1), (A0, B2) and in second step, whatever the outputs coming from AND gates will become inputs to the OR gate and finally this OR gate output is given as the one of the input to Ternary type OR gate. And for the next 3-AND gates similar processes is followed but inputs are (A1, B0), (A0, B1), (A2, B2), and whatever the output coming from this gate is given to OR Gate and the output of the OR gate is given to T-buffer and the output of these buffer is given as the second input to the Ternary OR gate.

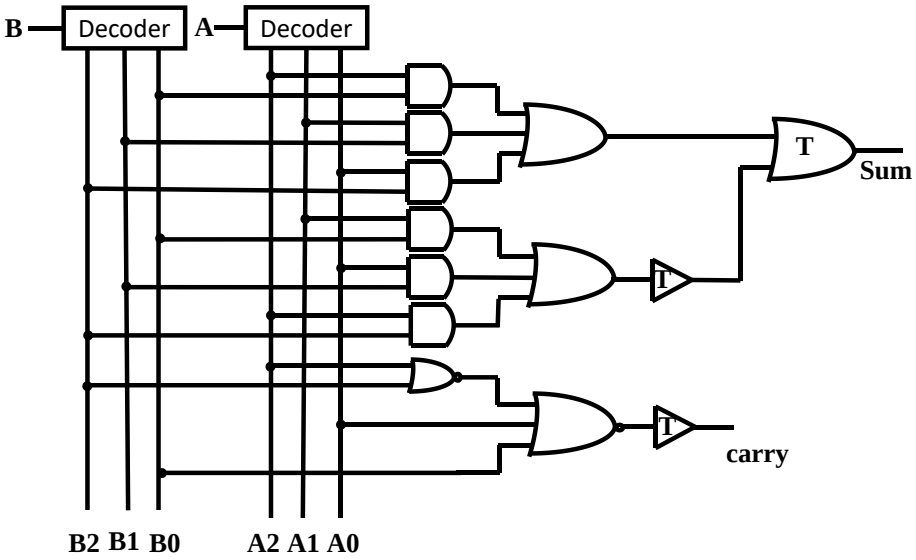

Figure 9. Ternary half adder

And finally, whatever the output we got form the Ternary OR gate will be our SUM. For carry operation, we implemented with the 2-NOR gates and one T-buffer gate, the inputs for the first NOR gate are (A2, B2), and the output of this NOR gate is taken as one of the input, to the second NOR gate and remaining inputs are (A0, B0). The output of this second NOR gate is given to Ternary(T)-buffer and out of this T-buffer will be our CARRY.

And from the truth table, Table 4 depicts we have different combinations of inputs (A, B) like (00, 01, 02) and for this inputs we have outputs like carry, Sum (00, 01, 02). And for the next combination inputs A, B (10, 11, 12), we have sum, carry as (01, 02, 10). similarly for the next combination of inputs A, B (20, 21, 22) we got the output like (02, 10, 11).

Table 4. Truth table of half adder

Input a	Input b	carry	sum
0	0	0	0
0	1	0	1
0	2	0	2
1	0	0	1
1	1	0	2
1	2	1	0
2	0	0	2
2	1	1	0
2	2	1	1

Table 5 depicts that for the sum and carry outputs, we have equations from the truth table and the equations are represented in the form of input A and B we have (8).

$$Sum = 1^* (A0B1 + A1B0 + A2B2) + 2^* (A0B2 + A1B1 + A2B0) \quad (8a)$$

$$Carry = (A1B2 + A2B1 + A2B2)^*1 \quad (8b)$$

Table 5. The simulated and calculated delay and power at volage 0.9 V

GNR	Voltage	Delay (ps)	Power (nW)
Half adder	0.9	3.0603E-11	7.4307E+09

3. SIMULATION ANALYSIS AND RESULTS

Case 1: The proposed CMOS DRG 7T SRAM is same as the conventional 6T SRAM in performing the operations [18]. The circuit as two inverters connected back-to-back, 2 NMOS transistors and 7th NMOS transistor is connected to the ground part of the back-to-back connected inverter unit. Seven NMOS transistor in the circuit is utilized to decrease the leakage currents in CMOS SRAM unit.

Figure 10 describes DRG NMOS is connected in leakage path from supply voltage to ground. DRG transistor is kept in low leakage path, where the path becomes idle during read and write operation in order to keep down the leakage for the fall down of the power. Additionally, added transistors is in on, when the segment is in use and remains off when segment is not in use. When the DRG transistor is working it operates same as 6T SRAM and when it is not working DRG transistor leakage path goes to ground. It also makes the nodes to ground which as 0 so that writing the data 1 becomes quick. When DRG is on, it is back to zero state. When DRG is in off state data remains same without any loss. Table 6 depicts that when two transistors are in off state which are connected in series leakage current reduction is easy. There is the stacking consequence which means the reverse biasing of the stacked transistors. Table 7 shows additionally, added transistors can be shared with other SRAM cells. Gated grounded transistor as a good impact on holding the data and good power utilization, delay though the extra area is utilized for the gated ground transistor. However, it occupies additional area because of gating, data can be hold accurately. DRG transistor is connected to row static random memory unit. Decoder is used to have better performance and sizing. Table 8 depicts that by the addition of extra NMOS transistor discharge current in the circuit are minimized which resulted in the lower power utilization. Though the area is increased it as shown the better results in terms of power and delay.

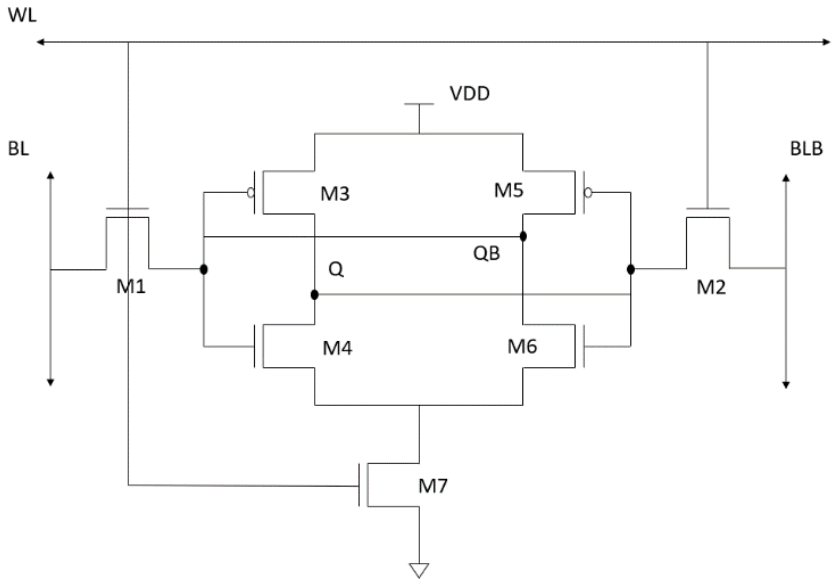

Figure 10. DRG 7T SRAM circuit

Simulations are performed in H-Spice tool under 32 nm technology. Figures 10-14 shows the Waveforms of the DRG 7T SRAM at 0.7 V, 0.8 V and 0.9 V, with x-axis voltage and y-axis as power. The following results are differentiated for conventional 6T SRAM and enhanced that the proposed DRG 7T SRAM as better results.

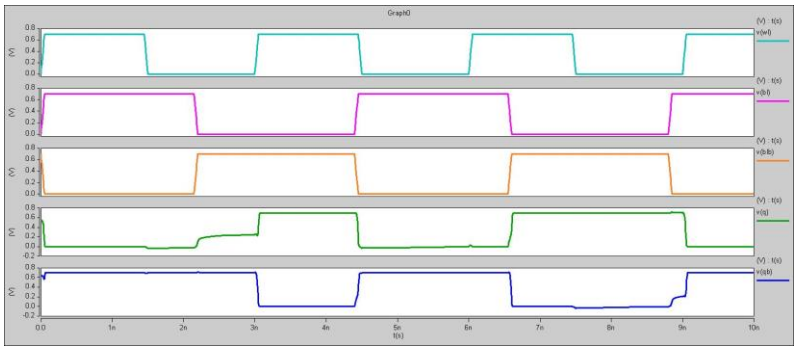

Figure 11. 7T 0.7 V SRAM Waveform

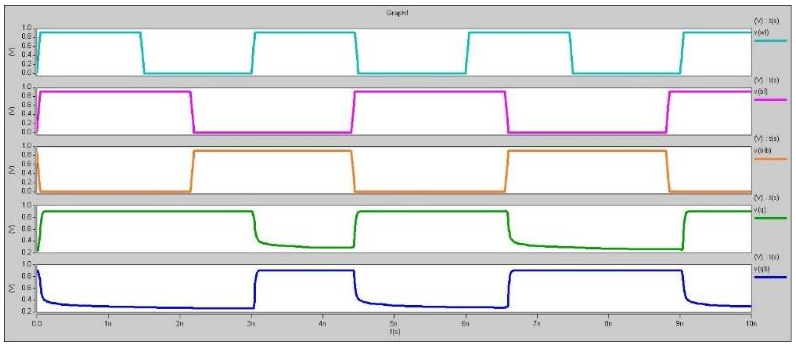

Figure 12. 7T 0.8 V SRAM Waveform

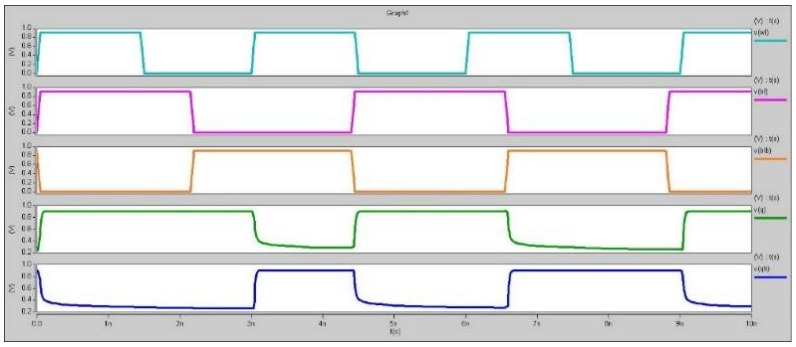

Figure 13. 7T 0.9 V SRAM Waveform

Table 6. Simulated results of the DRG 7T SRAM

Design analysis	Voltage (V)	Delay (ns)	Power (µW)
SRAM-32 nm DRG	0.7	0.44	2.5
SRAM-32 nm DRG	0.8	0.43	3.42
SRAM-32 nm DRG	0.9	0.41	4.8

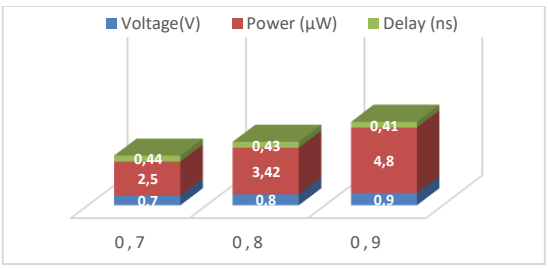

Figure 14. 7T SRAM static analysis

Case 2:-Figures 14-17 depicts that the proposed GNR DRG 7T SRAM is the same as the conventional 6T and 7T SRAM in performing the operations, Figure 18 depicts SRAM voltage with voltage under X-axis voltage and Y-axis power.

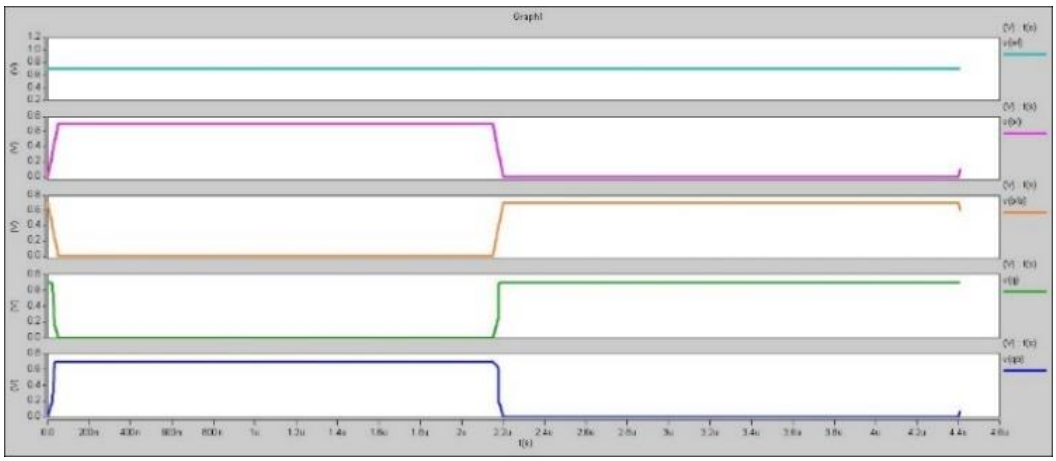

Figure 15. 7T 0.7 V SRAM Waveform

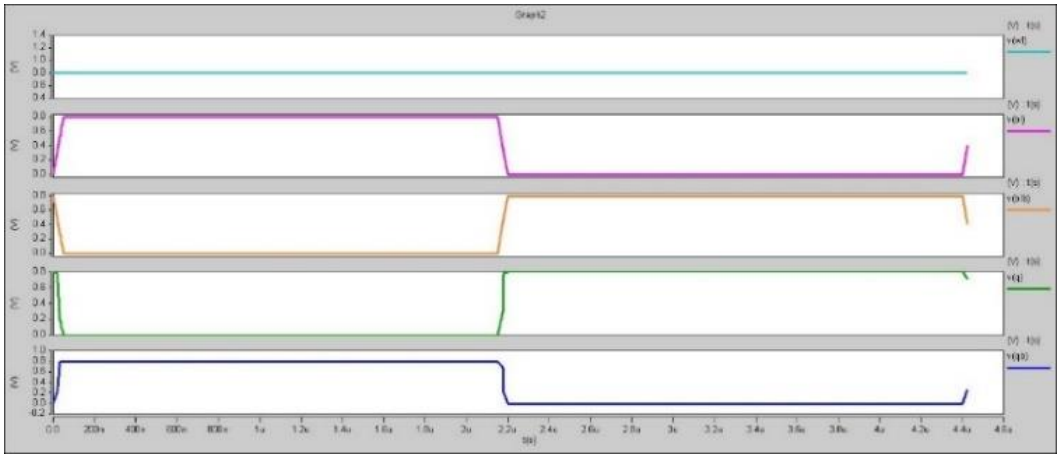

Figure 16. 7T 0.8 V SRAM Waveform

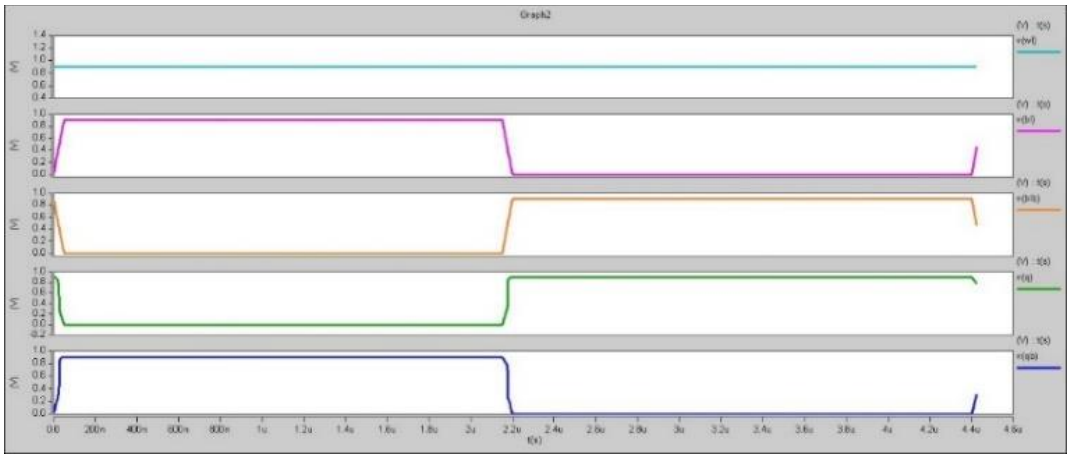

Figure 17. 7T 0.9 V SRAM Waveform

Table 7. Simulated results of the ternary DRG 7T SRAM in 32 nm technology

GNRFET SRAM	Voltage (V)	Delay (ns)	POWER (µW)
7T	0.7	3.77	0.28
7T	0.8	2.55	0.34
7T	0.9	1.25	0.53

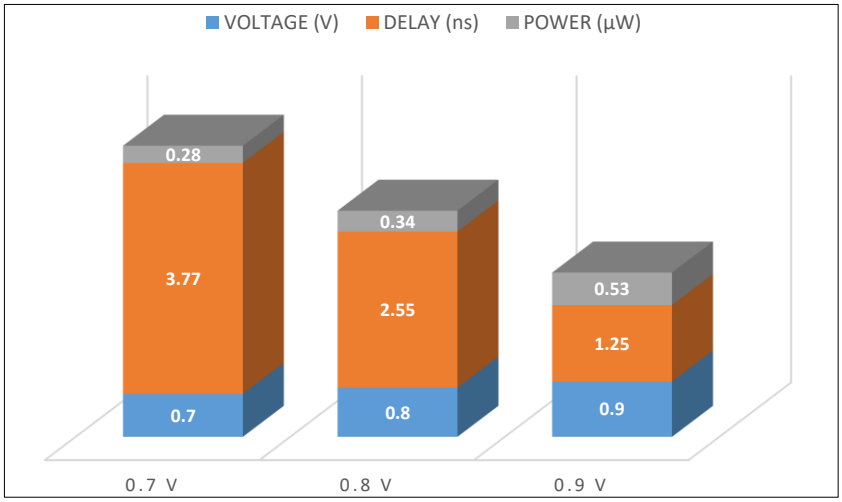

Figure 18. 0.9 V SRAM Waveform

Case 3:-Power delay product from Figures 18 and 19 x-axis depicts voltage and Y-axis of power delay it is observed that GNR power delay product is reduced when compared to with the conventional technologies.

The final output values of the DRG 7T SRAM under distinct voltage. The table shows the power, delay values at distinct applied voltages and proven that the proposed DRG 7T SRAM as better power and delay than conventional 6T SRAM. Finally, PDP improvements were noted at various voltages and integration of GNR characteristics at the nanoscale was improved in conductivity and decreased leakage.

Table 8. Power delay product for CMOS 6T,7T AND GNR 7T

PDP	CMOS 6T	CMOS 7T	GNR 7T
0.7V	1.30548E+17	1.1E+15	1.0556E+15
0.8V	3.17645E+17	1.4706E+15	8.67E+14
0.9V	5.55035E+17	1.968E+15	6.625E+14

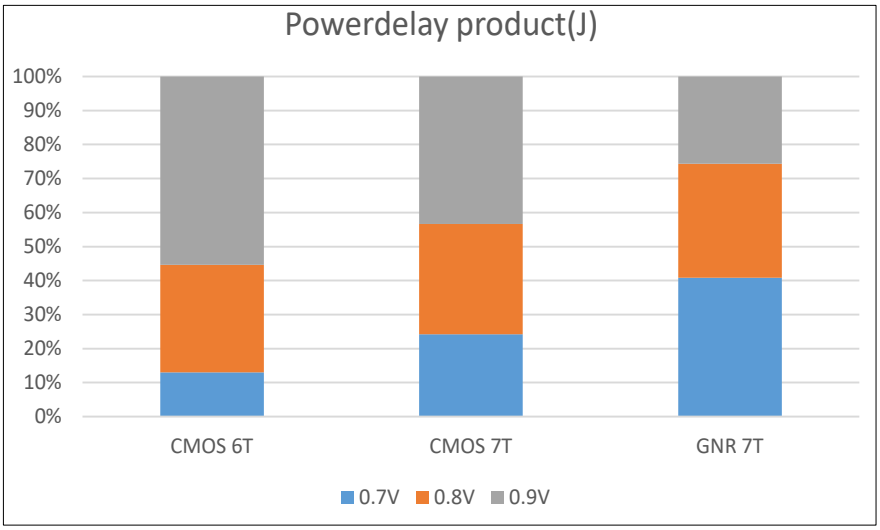

Figure 19. Power delay product for CMOS 6T, 7T AND GNR 7T

4. CONCLUSION

DRG SRAM with 7 transistors is proposed to decrease the power and delay compared to the CMOS 6T and 7T, compared the results of the SRAM at different voltages, and GNR 7T unit. Implementation is done in the H-Spice tool technology. The proposed DRG 7T SRAM consumes PDP of 1.055 E15 J AT 0.7 V, 8.67E14 J at 0.8 V, 6.625E14 J at 0.9 V, much less than the 6Transistor SRAM power delay product. Future developments in power and delay characteristics will be made possible by progressively reducing the physical footprint of SRAM. The design complexity and energy efficiency of SRAM cells can be maximized by utilizing cutting-edge field-effect transistor technology and new materials like GNRs.

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AUTHOR CONTRIBUTIONS STATEMENT

Name of Author	C	M	So	Va	Fo	I	R	D	O	E	Vi	Su	P	Fu
Ravikishore Gaddikoppula	✓	✓	✓	✓	✓	✓		✓	✓	✓				
Nandhitha Nathakattuvalasu Muthu		✓				✓		✓	✓	✓	✓	✓		

C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

No conflict of interest.

DATA AVAILABILITY

Data availability is not applicable to this paper as no new data were created or analyzed in this study.

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