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A high linearity low noise amplifier with modified differential inductor for bluetooth profiles

Ghattamaneni Usharani[1], Sourirajan Varadarajan[2]
Department of Electronics and Communication Engineering, S V University College of Engineering, Sri Venkateswara University, Tirupati, India

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ABSTRACT

In today's rapidly evolving communication landscape, electronic devices rely heavily on high-performance components to ensure seamless connectivity. A low-noise amplifier (LNA) is a critical front-end element in any receiver chain, where its performance significantly influences the overall system efficiency. As integrated circuits continue to shrink with advancements in technology, challenges such as linearity degradation have become increasingly prominent. This work presents a modified derivative (MD) narrowband common source low-noise amplifier (CSLNA) designed using 0.13 µm CMOS technology, offering improved linearity and frequency characteristics. The proposed design adopts a hybrid architecture, combining a folded cascode gain stage with a common-gate configuration. An optimized modified differential inductor is employed at the input for effective impedance matching and reduced noise figure (NF). The implemented LNA achieves a gain of 25.81 dB, an input return loss of –24.86 dB, and maintains a low NF of 0.3 dB at an operating frequency of 2.4 GHz. Furthermore, the linearity metrics-third-order input intercept point (IIP3) and 1 dB compression point-are significantly improved to –16.70 dBm and –21.89 dBm, respectively. These results highlight the LNA's suitability for Bluetooth and other short-range wireless communication applications.

Corresponding Author:

Ghattamaneni Usharani
Department of Electronics and Communication Engineering, S V University College of Engineering
Sri Venkateswara University
Tirupati, India
Email: usharani.svu2000@gmail.com

1. INTRODUCTION

Extensive research has focused on developing wideband multistandard receivers capable of concurrently demodulating multiple radio signals. A critical component in the receiver front-end is the low-noise amplifier (LNA), which significantly influences overall performance. Employing multiple narrowband LNAs to support various frequency bands for each communication standard can lead to increased system complexity, size, and cost-posing major design challenges. As a result, narrowband receivers are more efficiently coupled with narrowband LNAs [1]. To ensure high performance, the LNA must deliver a high gain, low noise figure (NF), and precise narrowband input impedance matching. Additionally, maintaining excellent linearity is crucial due to the presence of multiple closely spaced channels within the wide operating bandwidth [2]. Nonlinearities, such as second-order (IMD2) and third-order intermodulation distortion (IMD3), generated by the LNA, can significantly degrade the receiver's sensitivity and overall signal integrity [3]. Numerous techniques have been recorded to enhance the linearity of millimeter wave, broadband, and narrowband low noise amplifiers [4]-[9]. The common-source (CS) stage, utilizing diverse

topologies such current reuse, source degeneration, and cascode methods, can attain high gain and enhanced for narrowband applications while mitigating transconductance nonlinearity [10], [11]. The commongate (CG) amplifier configuration offers inherent narrowband matching, little power consumption, and notable linearity [12], [13].

However, a solitary CG stage cannot deliver adequate gain throughout the narrow band with the requisite flatness unless augmented by supplementary bandwidth extension technology. Conversely, the traditional CG-LNA and CS-LNA cannot guarantee a linearity [14]. The cascode has garnered significant research interest due to its intrinsic properties of delivering outstanding narrowband matching, linearity, and stability. Nonetheless, the NF of a common-gate LNA is typically elevated owing to the input matching requirement $g_m = 1/r_S$, where g_m represents the transconductance of the input transistors. In recent years, various feed-forward techniques for linearity improvement based on intermodulation distortion (IM3) cancellation have been proposed but these techniques effecting to the other parameters, this study investigated the effects of linearity [15], [16]. While earlier studies have explored the impact of power dissipation and input impedance matching, they have not explicitly addressed its influence on circuit complexity [17]. Wherein a signal of equivalent amplitude and inverse phase to IM3 is produced in an auxiliary pathway and introduced to the output of the primary pathway for cancellation and linearization [18].

A linearization method has been presented that generates a low-frequency second-order intermodulation to mitigate the third-order intermodulation. In the push-pull differential amplifier is integrated with a cross-coupled g_m gain to mitigate sensitivity to bias fluctuations [19]. The cascaded CS_LNA and CG_LNA technique having good gain but lesser bandwidth and fluctuations in linearity [20], the Darlington configuration with multi gated LNA require the more number of transistors but its having the more circuit complexity [21]. Jang *et al.* [22] presents a LNA using shunt feedback and current mirror loading, which elevates power dissipation owing to the requirement for an additional similar pathway. The transformer based interstage LNA [23] also require the more power. Guo *et al.* [24] examines the complementary CS-LNA utilizing an active inductor that incorporates feedback from a second-order nonlinear element derived from the decoupling inductance, which contributes to the third-order nonlinearity. A narrowband noise-canceling CMOS LNA with enhanced linearity by using complementary nMOS and pMOS configurations having the unstabilizedNoisefigure [25].

We found that linearity correlates with gain. This study proposes a modified derivative (MD) technique designed to provide enhanced linearity and stabilized gain characteristics without effecting the other parameters like gain and NF, the structure consist of folded cascode configuration and common source with split inductor. The Paper organized as follows section 2 discussion about the linearity enhancement of the proposed technique, the section 3discussion the result and analysis and section 4follows the conclusion and future scope of the proposed method.

2. PROPOSED DESIGN

It is essential to investigate novel approaches to attain high gain by combining a folded cascode with a gain boosting technique and a common-gate LNA that employs a split inductor to enhance linearity while ensuring sufficient input matching. The suggested circuit comprises three primary components: i) folded cascode LNA, ii) gain enhancement approach, iii) MA to improve the linearity.

2.1. Folded Cascode LNA

The folded cascode architecture offers an effective solution to the challenge of stacking multiple transistors in low-voltage environments. As shown in Folded cascode LNA Figure 1, this configuration utilizes a PMOS transistor (M2), while an NMOS transistor (M1). A supplementary current source, I2, is introduced to bias M2 and serve as its active load. The biasing of transistor M1 is defined by the current difference (I1 – I2). Additionally, a DC bias voltage, Vb, is applied to the gate of the cascode transistor M2 to ensure the correct operating point. This folded cascode-based LNA is particularly well-suited for low-voltage applications, enabling efficient operation without sacrificing performance. The corresponding small-signal model of the MOSFETs is depicted in Figure 1(a), providing a clear representation of the circuit's frequency response and gain behavior 1(b).

The circuit operates analogously to the NMOS cascode design under small-signal conditions. The phrase "folded cascode" derives from the fact that the signal current $g_m v_{gs}$ is redirected downward and enters the source terminal of M_2. The folded cascode is a frequently utilized element in CMOS amplifiers. For analytical reasons, the channel modulation effect and the back-gate effect of the folded cascode are typically disregarded. The folded cascode comprises two components: the common source (CS) and Common source (CG) LNA, with their respective small-signal models illustrated in Figures 1(b). The internal capacitors C_{gs1} and C_{gd1} are positioned near the sources and drains of M_1. The small-signal current produced by the input

transistor M_1 traverses C_{gd1}, C_{gs1}, and subsequently to ground, alongside the load resistor, leading to a reduction in gain as frequency increases. Illustration. Small signal model of the NMOS and PMOS in Figure1(b) The capacitors M_2, C_{gd2}, and C_{gs2} are crucial in setting bandwidth, with C_{gd2} often being smaller than C_{gs2}. Reducing the capacitance of M_2 enhances the bandwidth, which is beneficial. Nonetheless, diminishing the dimensions of M_2 results in a decrease in g_{m2}, which subsequently causes an escalation in leakage current attributed to C_{gd1}. Moreover, a reduced M_2 influences linearity and necessitates an increased voltage margin. When Vin decreases, I_{D2} similarly decreases, reaching zero if I_{d1} equals I_1. For this to occur:

$$I_1 = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_1 (V_{DD} - V_{in} - |V_{TH1}|)^2 \quad (1)$$

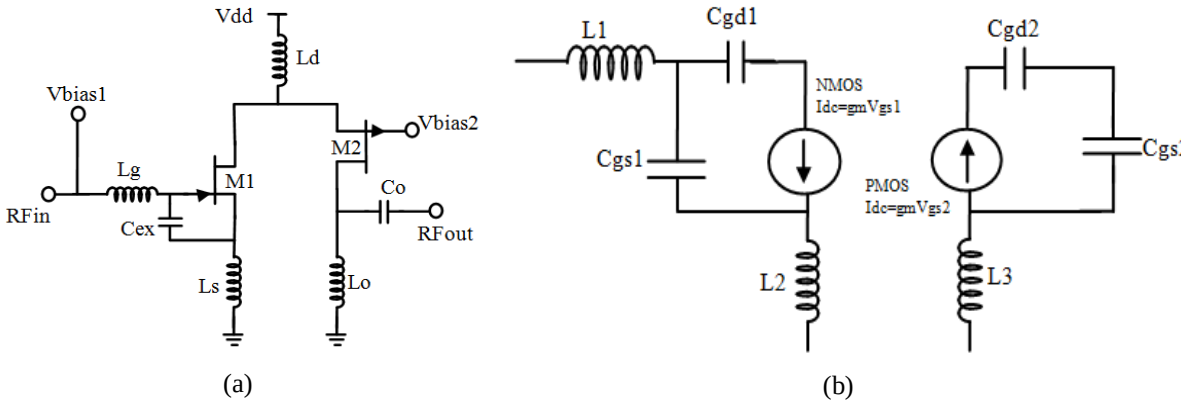

Figure 1. Folded cascode LNA and its small signal MOSFET (a) GeneralFolded cascodeLNA and (b) small signal model of MOSFET: NMOS and PMOS

2.2. Gain enhancement

Amplification of Gain To offset the restricted gain, gm-boosting techniques are employed in folded cascode arrangements to enhance signal intensity in Figure 2. An inverting amplifier is positioned between the source and gate terminals of the NMOS transistor M4 in proposed LNA Figure 2(a) ith a shared gate in these procedures. The incorporation of gm-boosting techniques in folded cascode topologies seeks to address the restrictions of gain constraints and enhance total signal gain [26].

2.3. Proposed method-modified derivative

The while previously discussed techniques—such as the folded cascode for bandwidth enhancement and the folded cascode with gain boosting—effectively improve specific performance metrics, they often compromise linearity. To address the degradation caused by third-order nonlinearities, particularly those stemming from the amplification of second-order distortions, advanced linearization techniques such as multiple gated transistors (MGTR) are implemented in the common-gate stage of the MD (MD) method. Figure 2(b) presents the complete MD configuration incorporating a folded cascode architecture, while Figure 3 demonstrates the resulting linearity improvements in comparison to the small-signal model. In this folded-cascode LNA topology, the MOS transistor and the degenerative inductor in the common-source stage are divided into two sub-stages (labeled MA and MB) to suppress third-order intermodulation distortion. Transistor MA is appropriately biased, whereas MB operates in strong inversion, as illustrated in Figure 3. The third-order nonlinearity in inductively degenerated LNAs is significantly influenced by second-order distortions introduced through feedback mechanisms. To combat this, the common-source stage of the LNA actively reduces third-order nonlinear effects by balancing the output currents of the main and auxiliary signal paths. This current equilibrium at the output nodes, as shown in Figure 2(a), effectively enhances linearity and ensures improved performance in short distance communication systems.

The second-order and third-order nonlinearities of the M_A and M_B transistors are designated as g_{m21}, g_{m22}, g_{m31}, and g_{m32}. The transconductance of the NMOS transistors M_B and M_A is designated as g_{m11} and g_{m12}, respectively. The second-order composite nonlinearities of M_A and M_B are expressed as $g_{m2} = g_{m21} + g_{m22}$, and the third-order composite nonlinearities are represented as $g_{m3} = g_{m31} + g_{m32}$.

The overall third-order nonlinearity is diminished by optimizing the operational parameters of the MOS transistors to ensure that the positive peak of g_{m31} coincides with the negative peak of g_{m32}, resulting in a composite third-order nonlinearity (g_{m3}) that is 180 degrees out of phase with the second-order nonlinearity

(g_{m2}) through the use of source degeneration inductance L_{blk}. The bias of the MOS transistor at the zero crossing of the third-order nonlinearity component (g_{m3}) rectifies the third-order nonlinearity. The integration of the composite third-order nonlinearity with the 180-degree phase-shifted effect of the second-order nonlinearity restricts the IMD3 contribution from the second-order nonlinearity through a split-inductor arrangement, hence enhancing IIP3 performance.

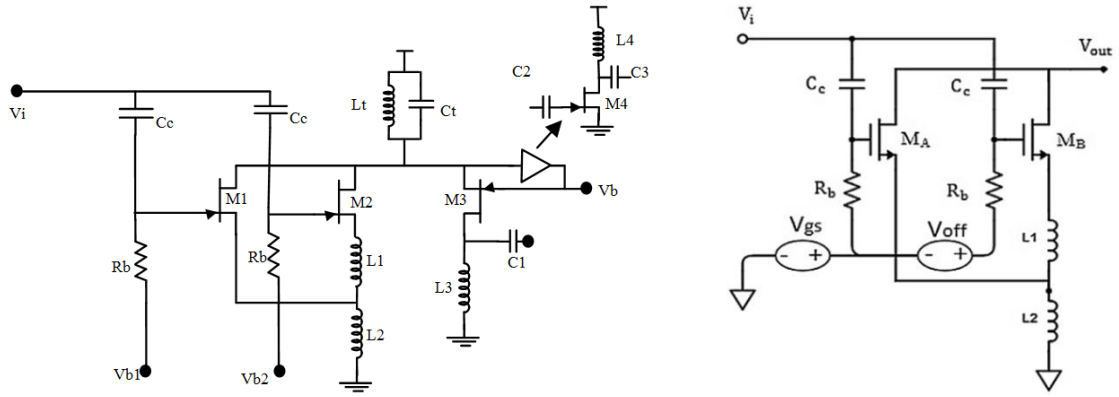

Figure 2. Small signal model of MOSFET (a) proposed folded cascode MD LNA and (b) MD

2.3.1. Matching input impedance

The small-signal model of the folded cascode MD LNA using a Π input matching network as shown on Figure 3. The Π-network configuration is used to align the input impedances with 50 ohms. The equation delineating the input impedance of the MD method is provided by (3).

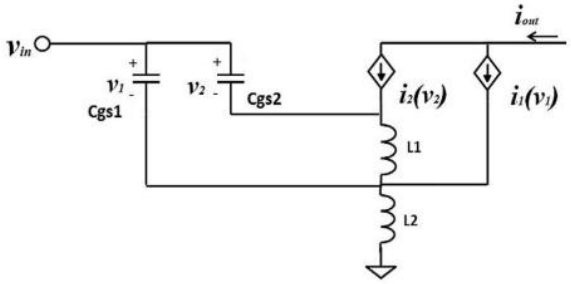

Figure 3. Input impedance matching network

$$Z_{in}(s) = s\left[\left(\frac{c_{gs2}}{c_{gs\tau}}\right)L_1 + L_2\right] + \frac{1}{sC_{gs\tau}} + \frac{g_{m11}L_2 + g_{m12}(L_1+L_2)}{C_{gs\tau}} \quad (3)$$

2.3.2. Linearity improvement

The linearity analysis encompasses the assessment of the non-linear currents produced by the compound MOSFETs employed in the MD architecture. Enhancing linearity necessitates the mitigation of third-order intermodulation distortion components. The third-order intercept point (IIP3), a critical parameter for assessing receiver performance in environments with significant interference, quantifies intermodulation distortion products. The two-tone test, a prevalent technique, determines the third-order intercept point by stimulating the LNA with two closely spaced frequencies, w_1 and w_2.

$$V_{out} = A\,[cos(w_1 t) + \cos(w_2 t)] \quad (4)$$

The coefficients are solved by the Volterra series

$$IIP_3 = \left(2w_2 - w_1 = \frac{1}{6Re(Z_{in}(S))}\left|\frac{4g_{m12}4g_{m12}^2w^2[L_2C_{gsT}+L_1C_{gs2}]}{|\varepsilon|}\right|\right) \quad (5)$$

$$\varepsilon = g_{m31}(1+jwL_1g_{m12})[1+(wL_1g_{m12})^2]\left[1+\frac{L_1C_{gs2}}{L_2C_{gsT}+L_2C_{gs2}}\right]+g_{m32}-\frac{2g_{m22}^2}{3g_{m22}}\left(\frac{j2wg_{m12}[L_1+L_2]}{1+j2wg_{m12}[L_1+L_2]}\right) \quad (6)$$

The input impedance is represented as $Z_{in}(S)$ in (5). The initial two terms in the equation denote the composite third-order nonlinearity g_{m31} in conjunction with g_{m32}, whereas the third term, g_{m22}, represents the second-order nonlinear component.

The word ε denotes the second-order nonlinear influence on the third-order nonlinearity. Analysis of (5) and (6) indicates that enhancing IIP3 necessitates the reduction of the third-order intermodulation nonlinearity component g_{m3}. The linearity is assessed using the 1 dB compression point and the IIP3 measurements. The suggested design exhibits a 1 dB compression point of -21.89 dBm and an IIP3 of -16.70 dBm. The introduction of currents in both the primary and auxiliary paths at the output nodes facilitates the attainment of linearity. This method efficiently mitigates the third-order nonlinearity distortion generated by the common source stage of the LNA.

2.3.3. Bandwidth boosting

A multistage amplifier circuits Their gain stages, a reactive impedance matching network, and an interstage network. The matching networks partially compensate for the transistors' gain reduction with frequency, resulting in a uniform gain response. Transistors can achieve flat gains by diminishing their low-frequency gain response. To mitigate the impact on the frequency response, the capacitance C1 in the circuit simulations is set to a gain-boosting of 1.1 pF. It effectively isolates the gate and drain DC bias of the transistor. The ultimate LNA design exhibits maximum gain across the frequency spectrum of 2.4 GHz. The frequency response has a steeper positive slope and a higher maximum gain. To obtain the correct frequency response, the circuit components must be carefully selected to take into account the frequency drop of the other amplifier stages.

2.3.4. NF improvement

Enhancement of NF Two adaptation strategies were employed to optimize the biasing of the initial stage transistor, hence enhancing the overall NF. An essential enhancement entails the incorporation of an inductance into the transistor's drain bias circuit to reduce the drain bias voltage. This modification results in a marginal rise in power consumption.

The swift decline in gain at elevated frequency ranges poses a difficulty for common source (CG) LNAs and leads to a deterioration of A Introduction Extensivees. By leveraging the increased gain of the CG stage at elevated frequencies, the AF contribution of the succeeding stage can be reduced. In (7) demonstrates this phenomenon, leading to a more uniform frequency response. The LNA's architectural design integrates passive structures and is optimized using electromagnetic (EM) simulations using ADS Momentum to guarantee although its performance and noise attributes.

$$F = 1+\frac{\gamma}{\alpha}(1-2|C|)\sqrt{\frac{\delta\alpha^2}{5\gamma}}+\sqrt{\frac{1+Q^2}{Q^2}}+\sqrt{\frac{w_0}{w_T}} \quad (7)$$

3. RESULTS AND DISCUSSIONS

This study investigated the effects of linearity in cascode structure LNA by adding the split inductor to reduce the second and third order hormonics. While earlier studies have explored the impact of gain and power consumption and circuit complexity, they have not explicitly addressed its influence on LNA stabilization. We found that linearity correlates with other parameters like gain, circuit optimization and operating voltage. The proposed method in this study tended to have an inordinately higher proportion of linearity with stabilized gain in Figure 4.

Figures 4(a) and (b) in the experiment illustrate the simulated measured S-parameters return loss (S_{11}) and voltage gain (S_{21}) of the LNA in the worst-case process, voltage and temperature (PVT) low-noises, including a standard process with a temperature range of -40°C to 120°C, and it illustrates the attainment of S_{11} at -24.86 dB and S_{21} at 25.81 ± 1.5 dB at 2.4 GHz within the frequency spectrum of 2 to 12 GHz.The gain and return loss are not flat as the given range of frequency, they are fluctuated at the 5-9GHz.A 3 dB bandwidth of 9 GHz is exhibited the common source configuration provides the proper input impedance marching it helps to improving the linearity. The 1dB compression point is roughly reaches to -21.89 dB, with an operating point 3 (OP3) of -3.65 dBm and an input intercept point 3 (IIP3) of -16.70 dBm as shown in Figures 4(c) and (d) is due effect of reducing the hormonics with split inductor structure by changing the phase shift of the signal.

The simulated NF of the LNA depicted in Figures 4(e) and (f), exhibits a gain variation with respect to rf power, it is saturation at origin and becomes low at when the power increases and minimal NF of 0.4 dB at 2.4 GHz and sustains low NF values from 2 to 12 GHz. The LNA is biased at V_{DD} = 0.7V and Vb = -0.5V. The important two measures for checking the linearity are the 1dB compression point and IIP3.

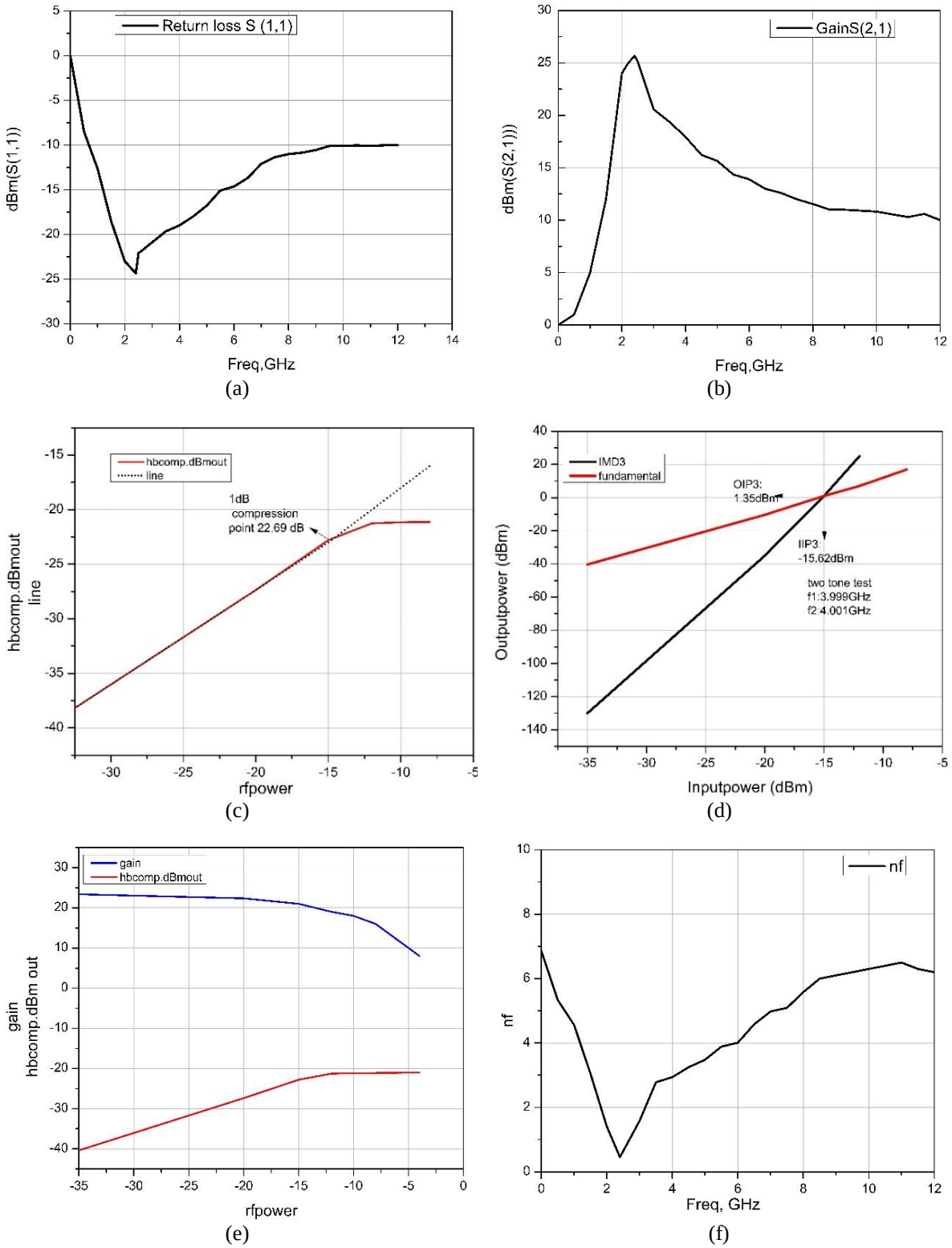

Figure 4. Simulation results of the proposed LNA: (a) return loss (S_{11}), (b) gain, (S_{21}), (c) 1dB compression, (d) IIP3, (e) power gain, and (f) noise figure

In comparison to analogous designs, the LNA provides a broad bandwidth of 9 GHz, with an average gain of 10 dB across the 2-12 GHz spectrum, reduced low-frequency noise, and notable linearity, as illustrated in Table 1. This study explored a comprehensive linearity with folded cascode LNA with common source and split inductor configuration. However, further and in-depth studies may be needed to confirm its improving the gain, especially regarding the limitation of this work is adding additional circuitry.

Table 1. Performance of proposed LNA with reported works

MethodeReference no.	Frequency (GHz)	Returnloss (S11) (dB)	Gain (S21) (dB)	BW (GHz)	Noise figure (dB)	1dB point (dBm)	IIP3 (dBm)	Voltage (V)	Technology (nm)
Dual band gain enhancement	2.4	-31.5	18	8	0.4	-25	-35.2	2.3	130
cascode LNA using tuned inductor	2.4	-17	17.89	7	0.5	-24	-33.4	1.3	130
cascode LNA, CG linearity enhancement	2.4	-16	19.90	8	2.6	-32	-36.1	1.42	130
Self-Bias Folded cascode LNA	2.4	-14	16	7	3.6	-25	-31.8	1.1	130
This method	2.4	-24.86	25.81	9	0.4	-21.89	-16.7	0.8	130

4. CONCLUSION

This study presents a 0.13-µm CMOS narrowband LNA design utilizing a folded cascode configuration. The Modified Differential (MD) approach is employed to enhance the Input Intercept Point 3 (IIP3) and attain 1 dB compression. The simulated findings indicate a beneficial gain at 2.4 GHz while preserving input and output matching over the full frequency band. The linearity measurements indicated an IIP3 value of -16.70 dBm and a 1 dB compression point of -21.89 dBm. The LNA functions with altered power provided from a 0.7 V source. The study's results indicate outstanding performance and confirm the appropriateness of the suggested narrowband LNA topology for applications necessitating narrowband functionality. The disadvantage of this technique is to require additional circuitry is split inductor with biased additional Common source configuration. This study explored a comprehensive linearity with gain only. However, further and in-depth studies may be needed to confirm its linearity improvement without effecting the bias voltage, especially regarding circuit complexity.

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AUTHOR CONTRIBUTIONS STATEMENT *(mandatory)*

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Name of Author	C	M	So	Va	Fo	I	R	D	O	E	Vi	Su	P	Fu
Ghattamaneni Usharani	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓	
Sourirajan Varadarajan		✓				✓		✓	✓	✓	✓	✓		

C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing -**O**riginal Draft
E : Writing - Review &**E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

Authors state no conflict of interest.

DATA AVAILABILITY

Data availability is not applicable to this paper as no new data were created or analyzed in this study.

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BIOGRAPHIES OF AUTHORS

Mrs. Ghattamaneni Usharani is IETE fellow member. She received B.Tech degree in Electronics and Communication Engineering from Jawaharlal Nehru Technological University, Hyderabad, India in 2008. She received M.Tech degree in Systems and Signal Processing from Jawaharlal Nehru Technological University, Hyderabad, India in 2014. She is currently pursuing Ph.D. Department of ECE, SVUCE, Sri Venkateswara University, Andhra Pradesh, Tirupati, India. Her research interests include VLSI design for wireless communication systemsand Bluetooth Receivers. She can be contacted at email: usharani.svu2000@gmail.com.

Prof. Sourirajan Varadarajan received M.Tech degree from NIT, Warangal and Ph.D. from Sri Venkateswara University, Tirupati. Former Secretary State Council of Higher Education, Andhra Pradesh. Currently, he is a Professor at Sri Venkateswara University College of Engineering, Tirupati. He established the Centre of Excellence (CoE) laboratory for Atmospheric Remote Sensing and Advanced Signal Processing. His research interests include atmospheric radar signal processing, Antenna System designing and communication networks." He can be contacted at email: varadasouri@gmail.com.