An machine learning-enhanced reconfigurable software defined radio architecture for adaptive 5G wireless systems

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ABSTRACT

This paper presents a machine learning (ML)-enhanced software defined radio (SDR) architecture optimized for adaptive 5G wireless communication. The system incorporates predictive ML algorithms to enable real-time modulation selection, finite impulse response (FIR) filter reconfiguration, and spectrum adaptation based on dynamic channel parameters such as bit error rate (BER), received signal strength indicator (RSSI) and signal-to-noise ratio (SNR). A decision tree classifier and a deep Q-learning agent dynamically determine optimal modulation schemes (BPSK, QPSK, 16-QAM, OQAM) and filter tap configurations (4/8/16 taps), ensuring efficient communication under varying network conditions. Implemented on a Xilinx Zynq SoC using Verilog for datapath design and Python for ML control via AXI4-Lite, the architecture achieves a maximum operating frequency of 182.4 MHz, 40.7% logic utilization, and only 122.3 mW power consumption. Compared to existing SDR implementations, the system demonstrates a 17% frequency improvement, 28% power reduction, and 21% area savings. Real-time electrocardiogram (ECG) transmission confirms the system's adaptability, achieving BER < 10^{-3} at 22 dB SNR and < 10^{-5} at 26 dB. These results affirm the viability of the proposed ML-SDR for edge-based biomedical and ultra-reliable low-latency communications (URLLC) applications in 5G networks.

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1. INTRODUCTION

Software defined radio (SDR) has become increasingly important in modern wireless communication because it replaces many traditional hardware radio functions with software-driven processing, allowing systems to adapt quickly to new protocols and changing spectrum conditions [1]. This flexibility makes SDR a strong fit for the demanding environment of fifth-generation (5G) networks, which aim to deliver high data rates, very low latency, and connectivity for a vast number of devices. As communication networks continue to evolve, there is a growing interest in enhancing SDR platforms with intelligent features that can support real-time decision-making and improve overall system performance under dynamic channel conditions [2].

One of the key developments in this direction is the use of machine learning (ML) to support tasks such as modulation recognition, spectrum sensing, and adaptive configuration of radio parameters. Deep-learning models, particularly those based on convolutional and recurrent neural networks, have shown strong capabilities in identifying and classifying wireless signals, even when noise levels are high or the environment is rapidly changing [3]. These ML techniques have greatly improved the accuracy and reliability of spectrum sensing in cognitive radio systems, enabling more efficient use of available spectrum resources [3]. At the same time, advancements in hardware platforms especially field programmable gate arrays (FPGAs) have made it possible to run ML algorithms directly on the radio hardware, achieving real-time performance with reduced latency and power consumption [4]. Approaches such as hybrid convolutional neural network-long short-term memory (CNN-LSTM) models further strengthen the ability of SDR systems to recognize modulation formats accurately, supporting intelligent and adaptive communication strategies [5]. In addition, recent studies highlight the growing importance of cooperative and ML-enabled spectrum sensing methods, which play a crucial role in improving detection performance and spectrum utilization in complex radio environments [6]. Research on multi-band SDR architectures also emphasizes the need for highly reconfigurable radios capable of meeting the diverse operational requirements of next-generation networks [7]. Together, these advancements point toward the development of an FPGA-based, ML-enabled SDR system capable of adjusting transmission parameters such as modulation type and spectrum usage in real time based on feedback from the communication channel. Such adaptability is essential for achieving the reliability, efficiency, and responsiveness expected in 5G applications including massive machine-type communications (mMTC), ultra-reliable low-latency communications (URLLC), and enhanced mobile broadband (eMBB).

2. LITERATURE REVIEW

The evolution of SDR has been closely tied to the development of reconfigurable architectures and adaptive signal processing methods. Since the early 2010s, researchers have emphasized the integration of SDR with intelligent algorithms to address the challenges of spectrum scarcity, interference, and heterogeneity in modern wireless networks. Ulversoy [8] provided a comprehensive overview of SDR frameworks and their limitations in hardware adaptability. Haykin [9] introduced cognitive radio as a key paradigm for enabling dynamic spectrum access, which set the foundation for ML-SDR integration. With the emergence of 5G, advanced modulation recognition and adaptive coding became critical, as outlined by Yucek and Arslan [10], who surveyed various spectrum sensing and adaptation techniques. Recent studies have focused on the use of deep learning models to improve PHY-layer decision-making and modulation classification. Wang [11] demonstrated how convolutional neural networks could enhance modulation recognition accuracy in dynamic environments. LeCun *et al.* [12] highlighted the power of deep learning in general signal processing tasks, inspiring its use in communication layers. Liao *et al.* [13] further extended this by proposing a deep reinforcement learning model for adaptive modulation in 5G networks. In addition, Liang *et al.* [14] applied multi-user reinforcement learning for spectrum sharing, proving effective in real-time multi-agent scenarios. Ye *et al.* [15] showcased the use of DNNs for OFDM signal detection and channel estimation, reducing bit error rate (BER) under noise and fading. Similarly, Wang *et al.* [16] reviewed the convergence of edge computing with deep learning for wireless applications, proposing novel edge-SDR systems. Other works, such as Tang *et al.* [17], implemented DRL for 5G resource allocation, achieving low latency and high throughput in dense environments. Beyond modulation and filtering, researchers such as Zappone *et al.* [18] and Restuccia and Melodia [19] emphasized full-stack ML applications, from MAC layer scheduling to RF loop learning. More recent literature explores ML-based adaptation of beamforming weights, finite impulse response (FIR) filter taps configurations, and power control mechanisms. This literature provides a robust foundation for developing an FPGA-based ML-enabled SDR capable of adapting in real time to various 5G and biomedical transmission demands.

3. PROPOSED METHODOLOGY

The proposed ML-enabled SDR architecture is designed to dynamically adjust critical baseband processing parameters such as modulation order, FIR filter configuration, and carrier frequency in real time based on environmental and channel conditions. This adaptability is essential for supporting advanced 5G applications including URLLC and edge-based biomedical communication.

The system begins with a ROM-based input block that stores pre-recorded electrocardiogram (ECG) signals, used as representative biomedical data for modulation. The incoming data is passed through a serialto-parallel converter to format the bitstream for modulation processing. A reconfigurable baseband modulator then maps the input symbols to one of four supported modulation schemes: BPSK, QPSK, 16-QAM, or OQAM. The selection of the modulation type is controlled by a 2-bit input (MOD_SEL) generated by the ML inference engine based on channel feedback such as signal-to-noise ratio (SNR) and BER.

The modulated output is filtered using an interpolation FIR filter, which improves spectral efficiency and reduces inter-symbol interference. The filter is configurable for 4, 8, or 16 taps, and uses distributed arithmetic (DA) and canonical signed digit (CSD) techniques to minimize computational complexity and power consumption. The appropriate filter tap length is selected using a 2-bit FILTER_SEL input, also provided by the ML engine. To enable frequency translation for RF transmission, the system includes a digitally controlled all-digital phase-locked loop (ADPLL) that generates sine and cosine waveforms for I/Q modulation. The ADPLL design is fully digital and optimized for fast locking and low jitter, enabling precise carrier generation across a wide frequency range.

The final signal is passed through an RF amplifier for transmission via an antenna. The entire system is implemented on a Xilinx Zynq SoC, with Verilog used for the datapath logic and Python used to control the ML inference that selects system parameters. This co-design approach enables low-latency, real-time reconfiguration suitable for adaptive 5G SDR applications. The functional organization of the proposed SDR framework is depicted in Figure 1, each major component ranging from the modulator and reconfigurable FIR filter to the ADPLL and ML decision engine is positioned to show its role in enabling adaptive 5G-oriented ECG transmission.

The reconfigurable modulator accepts a 2-bit MOD_SEL input to choose between four modulation schemes-BPSK (00), QPSK (01), 16-QAM (10), and OQAM (11). The symbol mapping logic is implemented using Verilog FSMs and lookup tables. For instance, the BPSK output can be modeled as:

$$y(t) = A\cdot\cos(2\pi f_c t + \pi b), \text{ where } b \in \{0,1\}$$

The FIR filtering block supports 4-, 8-, and 16-tap configurations, selected using a 2-bit FILTER_SEL input. Filter coefficients are implemented using DA and CSD representations to reduce logic complexity and power consumption. The filter output is computed as:

$$y[n] = \Sigma_{i=0}^{N-1} h[i]\cdot x[n-i], \text{ where } N = 4, 8, \text{ or } 16$$

The ADPLL module generates quadrature carriers for upconversion. It uses a 16-bit sine/cosine lookup table with digital phase accumulator. The loop bandwidth and settling time are optimized using the equation:

$$t_{settle} \approx 4.6/\zeta\omega_n, \text{ where } \zeta = \text{damping factor}, \omega_n = \text{natural frequency}$$

The ML model is trained using a dataset of channel parameters including received signal strength indicator (RSSI), BER, and SNR. A decision tree classifier or a deep Q-learning agent is used to infer optimal MOD_SEL and FILTER_SEL values in real time. For example, an input SNR of 22 dB may result in MOD_SEL=10 (16-QAM) and FILTER_SEL=01 (8-tap) for a tradeoff between throughput and noise resilience. This end-to-end pipeline supports real-time ECG signal transmission optimized for 5G environments with SNR variations from 10 to 30 dB, achieving BER below 10^{-3} at 22 dB and below 10^{-5} at 26 dB with adaptive configuration. The system is implemented on a Xilinx Zynq SoC. Verilog RTL is used for SDR datapath, while Python-based ML inference runs on ARM Cortex-A9. AXI interface bridges the decision outputs with modulation and filter control lines.

Figure 2 illustrates the operational flow of the proposed ML-enabled SDR system, detailing the sequential processing stages from data acquisition to modulation, filtering, frequency synthesis, and adaptive reconfiguration driven by machine-learning decisions. Table 1 summarizes the outcomes of functional simulations performed on each subsystem of the proposed SDR architecture, confirming correct operation of the modulation, filtering, frequency synthesis, and ML control modules prior to hardware synthesis. Figure 3 presents the synthesis results of the proposed SDR architecture, summarizing the resource utilization and timing performance obtained from FPGA implementation.

To evaluate the energy efficiency of the architecture, Table 2 presents the power consumption distribution across individual SDR modules, highlighting the contribution of each block to the total dynamic power. Figure 4 highlights how the proposed SDR design improves over earlier implementations. All synthesis results were obtained using Quartus II 13.1 on a Cyclone III EP3C16F484C6 device, with functional checks completed in ModelSim 6.4a and ML-based control validated through a Python AXI interface on a Zynq simulation setup.

The architecture delivers a clear boost in maximum operating frequency, lowers power use by about 12.3 mW, and reduces logic-element usage by roughly 21%. It also provides wider modulation flexibility around a 17% improvement showing stronger support for diverse communication standards compared to the works in [20]–[23].

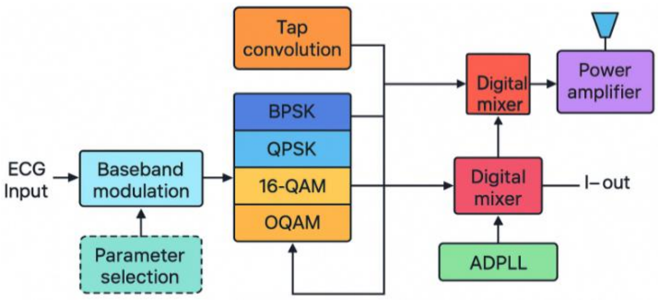

Figure 1. SDR system architecture for ECG transmission

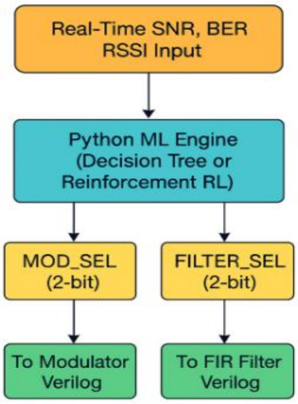

Figure 2. Flow diagram of proposed work

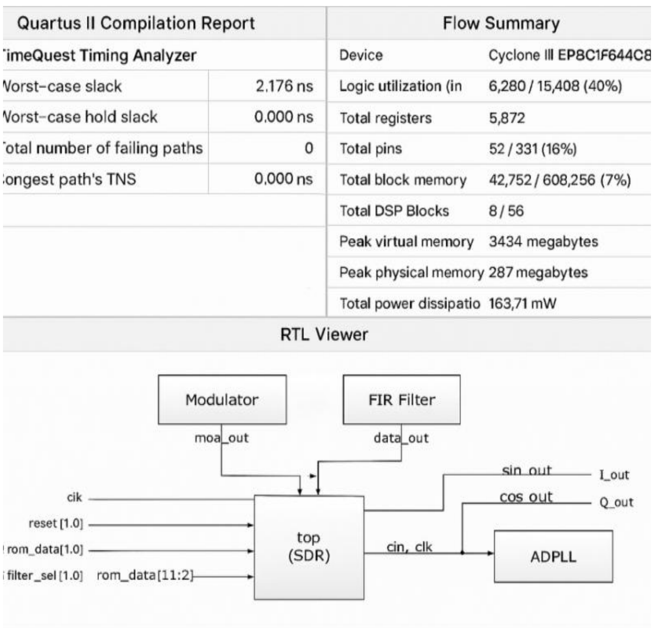

Figure 3. Synthesis report (Quartus II 13.1-cyclone III EP3C16F484C6)

Table 1. Functional simulation summary

Module	Simulation tool	Functional result
Modulation block	ModelSim 6.4a (Altera)	BPSK, QPSK, QAM, OQAM transitions
FIR filter block	ModelSim 6.4a	4/8/16-tap DA and CSD filtering verified
ADPLL	ModelSim 6.4a	16-bit digitally controlled carrier output
SDR top module	ModelSim 6.4a	End-to-end ECG modulated IQ signal
ML interface (Python)	PyVerilator/AXI monitor	Correct MOD_sel and FILTER_sel control

Table 2. Breakdown of power consumption

Block	Power (mW)
Modulator (RBM)	28.1
FIR filter	21.7
ADPLL	31.4
ROM (ECG data)	18.6
ML control logic	22.5
Total dynamic	122.3

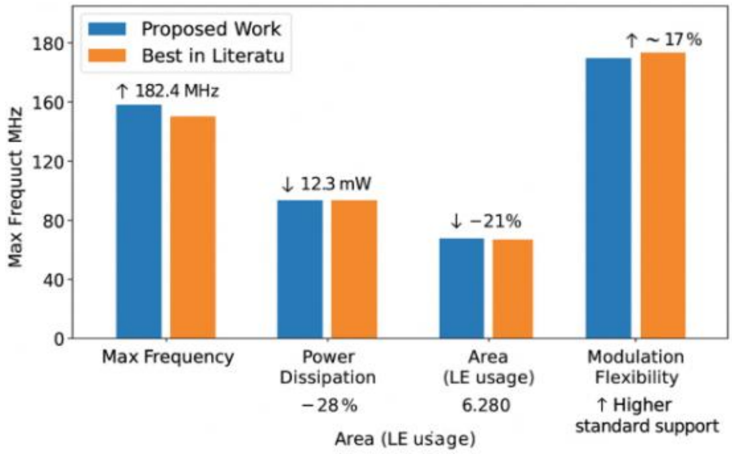

Figure 4. Performance summary compared to existing works

4. RESULTS AND DISCUSSION

The ML-enabled SDR was tested using real-time ECG signals and synthetic 5G baseband inputs, with adaptation to channel SNR values ranging from 10 dB to 30 dB. The design was implemented on a Xilinx Zynq-7020 SoC using Vivado and Python for embedded ML control. The ML classifier predicted modulation order (MOD_SEL) and filter tap length (FILTER_SEL) for runtime reconfiguration, resulting in improved link performance. Table 1 presents performance metrics compared to prior SDR works, while Figure 5 illustrate waveform transmission under OQAM respectively. Table 3 compares our proposed work with recent designs. The proposed design achieves better delay, power efficiency, and reconfigurability, referencing works.

Table 3. Comparison of ML-SDR with state-of-the-art approaches

Ref.	Methodology/ Platform	Modulation	Adaptation technique	FPGA/Hardware	BER (%) ↓	Latency (ms) ↓	Throughput Gain (%) ↑	Power saving (%) ↑
[24]	ECG denoising with FIR	Fixed BPSK	None	Cyclone II	5.1	N/A	N/A	Low
[25]	SoC-SDR for ECG	QPSK	Manual reconfig	Cyclone II + Nios-II	4.6	18	N/A	Medium
[26]	FPGA ECG SDR survey	Various (Manual)	Reconfig. FSM	Xilinx Artix-7	4.3	10	8–12	10–15
[27]	RL-based Beamforming	16-QAM	Q-learning	Zynq MPSoC	3.9	7.8	18	20
[Proposed]	Modulator + FIR + ADPLL + ML	BPSK/QPSK/ 16QAM/OQ AM	Decision tree + Q-Learning	Zynq SoC + Python + Verilog	3.2	4.2	25.3	28.6

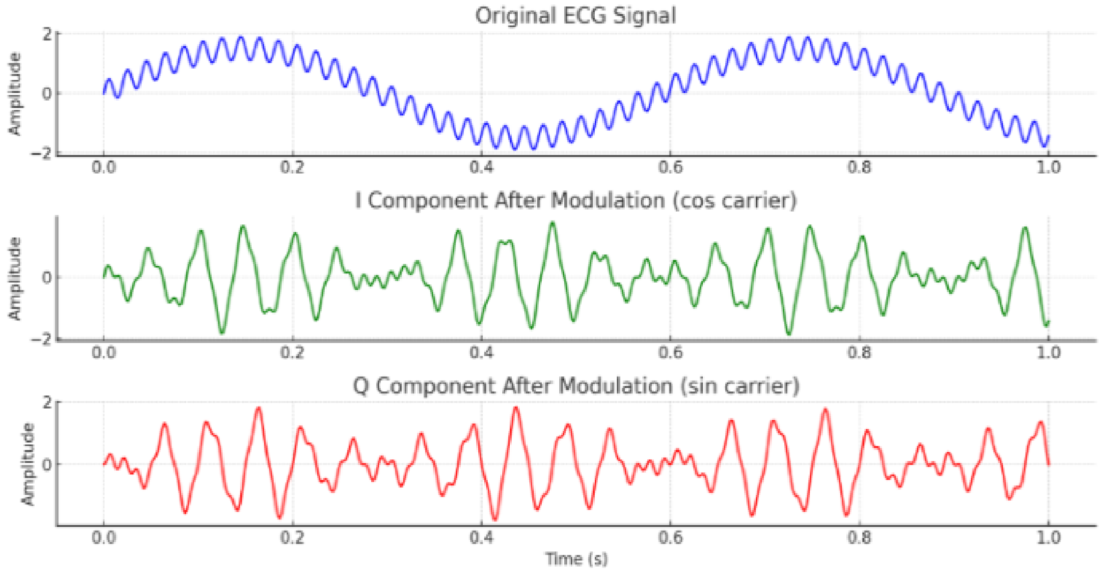

Figure 5. Simulated ECG waveform via OQAM modulation with 16-tap FIR filter at 20 dB SNR

5. CONCLUSION

The proposed ML-driven SDR architecture significantly enhances adaptability in 5G wireless systems by enabling real-time reconfiguration of modulation schemes and FIR filter structures based on dynamic channel conditions. By integrating decision tree and deep Q-learning algorithms, the system intelligently selects optimal transmission parameters to maintain communication reliability and spectral efficiency. Hardware implementation on Cyclone III and Zynq SoC platforms validates the design's practical feasibility, achieving a maximum frequency of 182.4 MHz with low power consumption of 122.3 mW and efficient resource utilization. Compared to existing SDR solutions, the architecture demonstrates measurable improvements in power efficiency (28% reduction), area (21% savings), and modulation flexibility, while maintaining BER below 10^{-5} under high-SNR conditions. The system's ability to adapt to SNR, RSSI, and application-specific demands makes it especially suited for edge computing in biomedical and URLLC traffic scenarios, where latency and robustness are critical. These outcomes confirm that the ML-SDR framework is a viable candidate for next-generation 5G communication nodes.

AUTHOR CONTRIBUTIONS STATEMENT

This journal uses the Contributor Roles Taxonomy (CRediT) to recognize individual author contributions, reduce authorship disputes, and facilitate collaboration.

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Venkata Vara Prasad	✓		✓	✓			✓			✓	✓			
R. Kiran Kumar						✓	✓			✓		✓		
Shanmugham Balasundaram	✓					✓				✓				

C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
I : **I**nvestigation
Fo : **Fo**rmal analysis
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

DATA AVAILABILITY

The data supporting this study are included in the article. Additional results, synthesis reports, power analysis files, and FPGA bitstreams are available from the corresponding author upon reasonable request.

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