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Design and analysis of low-k dielectric TSV liners for noise mitigation in high-frequency 3D ICs

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ABSTRACT

Moore's Law has driven the development of very large-scale integration (VLSI) technology, allowing continuous transistor scaling to increase speed, density, and performance. However, as two-dimensional (2D) integrated circuits (ICs) near their physical and performance boundaries, and 2.5D ICs still face interconnect delay and power issues, three-dimensional (3D) integration has become a practical solution. In 3D ICs, multiple active layers are vertically stacked and connected via through-silicon vias (TSVs), providing short, high-bandwidth interconnects between layers. Electrical TSVs are essential for signal transmission, but also cause noise coupling between adjacent TSVs, where an aggressive TSV can induce interference in a nearby TSV. This coupling can impair signal integrity, increasing delay and power consumption. To mitigate this, low-dielectric-constant (low-k) materials are used to reduce capacitive coupling. In this study, materials such as benzocyclobutene (BCB), Perylene-N, and Teflon AF 1600 are compared with conventional SiO_2. Generally, TSVs are two structures — single-liner and stacked-liner — which are analysed at 10 GHz and 1 THz frequencies. At 10 GHz, the single-liner structure incorporating SiO_2 exhibits a noise reduction of about 6.56 dB, whereas the stacked-liner configuration using Teflon AF 1600 provides a noticeably greater reduction of 8.40 dB. As the operating frequency increases to 1 THz, the advantage of the low-k dielectric becomes more evident, yielding 9.63 dB noise reduction for the single-liner and 12.04 dB for the stacked-liner structure. These results indicate that low-k materials effectively suppress capacitive coupling and mitigate high-frequency interference in 3D ICs. The stacked-liner design contributes additional isolation by creating a secondary dielectric barrier, which further minimizes electric field interaction between neighboring interconnects. Thus, the integration of low-k dielectrics with optimized liner architectures significantly enhances signal integrity and overall electromagnetic performance in advanced high-frequency 3D IC systems.

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1. INTRODUCTION

Over the past several decades, Moore's Law-the empirical observation that the number of transistors on a chip doubles roughly every two years-has served as the cornerstone for continuing progress in very large

scale integration (VLSI) technology. Scaling down transistor dimensions has enabled enhanced performance, lower power consumption, and higher integration density [1]–[3]. Yet, as device dimensions enter the deep nanometer regime, planar two-dimensional (2D) integrated circuits (ICs) increasingly confront fundamental limitations: interconnect delays, parasitic capacitances, rising resistances, heat dissipation, and signal-integrity degradation [4]–[6]. To partially mitigate these limitations, 2.5D integration was introduced. In 2.5D, discrete dies (chips) are placed side by side and connected via an interposer (e.g., silicon interposer) or redistribution layers (RDLs) [6]–[9]. While 2.5D offers improvements in bandwidth and modular integration, it still suffers from relatively long interconnect paths, limited vertical communication, and residual latency and power overheads-especially when bridging large lateral distances.

Consequently, three-dimensional (3D) integration has gained attention as a promising evolution. In 3D ICs, multiple active device layers (dies) are vertically stacked and interconnected by through-silicon vias (TSVs) [10]–[12]. These vertical interconnects drastically shorten signal path lengths, improve bandwidth, and enable finer-grained heterogeneous integration (e.g., logic atop memory) with reduced footprint and lower latency [13]–[15].

However, electrical TSVs bring their own set of challenges. At high frequencies, the relatively high dielectric constant of SiO_2 increases parasitic capacitance, leading to significant capacitive coupling and crosstalk noise between adjacent TSVs. This limitation motivates the use of low-k dielectric materials, which effectively reduce coupling effects and improve signal integrity in 3D ICs. A major hurdle is noise coupling (crosstalk) between adjacent TSVs: the switching activity in one TSV (the "aggressor") can capacitively or inductively couple unwanted signals into its neighbour (the "victim") [16]. This coupling leads to signal distortion, propagation delay, and degradation in reliability, particularly at high frequencies [17].

To reduce such interference, designers often opt for low-dielectric-constant (low-k) materials as insulating liners or dielectrics between TSVs. By lowering the dielectric constant, the parasitic capacitance-and hence coupling-can be reduced [18]. Conventional SiO_2 is widely used, but new dielectric materials such as benzocyclobutene (BCB), Perylene-N, and Teflon AF 1600 have attracted attention due to their lower permittivity and favourable electrical isolation characteristics [19]. Beyond material choices, the structural design of the TSV isolation is also vital. Two common TSV liner configurations are the single-liner and the stacked-liner (dielectric–metal–dielectric) structures [20]. These different arrangements influence the coupling paths and shielding effectiveness, especially at high frequencies.

In this work, we analyse and compare the noise-coupling performance of single-liner and stacked-liner TSV structures at 10 GHz and 1 THz using dielectric materials including SiO_2, BCB, Perylene-N, and Teflon AF 1600. Our results quantify the noise-suppression effectiveness (in percentage and dB) for each configuration, thereby highlighting the merits of low-k materials and advanced liner designs in 3D IC systems.

2. LITERATURE SURVEY

Vempalle and Dhal [21] experimentally investigate the use of BCB as a polymer filling/liner for high-aspect-ratio annular trenches used in TSV fabrication. The paper reports BCB's low dielectric constant, chemical resistance, and high thermal stability after curing - properties that reduce TSV capacitance and improve electrical isolation compared to conventional SiO_2 liners. The work also discusses processing challenges and demonstrates BCB's viability for dense TSV arrays. Although primarily a thermo-mechanical reliability study, Jung *et al.* [22] compare SiO_2 and polymer liners (including BCB) for TSVs and show that BCB's much lower Young's modulus reduces stress concentrations at the TSV/liner interface. The paper is important because it links liner mechanical properties to both reliability and the electrical performance tradeoffs when replacing SiO_2 with softer, low-k polymers [23].

Zhong *et al.* [24] develop lumped-circuit and scattering-parameter (S-parameter)-based models for TSV-to-TSV coupling, quantifying how dielectric parameters and TSV geometry influence crosstalk. While the paper uses SiO_2 in many baseline models, its modelling approach is directly applicable to the study of alternative liners such as BCB. It is frequently cited by subsequent material-focused studies. This parametric electromagnetic study systematically analyses how TSV geometric and material parameters (including SiO_2 liner thickness and different dielectrics) affect interposer and TSV crosstalk. The paper provides design guidelines to minimise capacitive coupling and illustrates the significant roles that the dielectric constant and liner configuration play at multi-GHz frequencies [25].

This study characterises the thermal and electrical behaviour of TSVs with BCB liners. Results show reduced TSV capacitance and improved high-frequency isolation compared to SiO_2 liners. However, the authors warn about trade-offs in thermal conduction (polymer liners reduce thermal paths) and recommend design measures for heat removal in stacked dies. The paper is useful because it quantifies the electrical benefits alongside thermal penalties [26].

3. DESIGN PARAMETERS

To minimise ambient interference during the integration of 3D ICs, multiple models are employed across various chips. Finished the use of through-silicon vias (TSVs), 3D ICs align chips by stacking them both electrostatically and vertically. The current focal point within 3D ICs utilising TSVs lies in the performance-to-clamour-coupling ratio of the system. TSVs are essential for 3D ICs to establish communication with other active devices. An issue arises when the TSV of the affected chip picks up the electrical signal path TSV's clamour. Research demonstrates that substituting the core materials for different liners can decrease crosstalk coupling between the electrical TSV (ETSV) and the affected TSV, as well as between the TSV and silicon. The strong connection between the TSV and the afflicted TSV is confirmed and studied. In accordance with the international technology roadmap for semiconductors (ITRS) roadmap, the normal pitch, which is the distance between TSVs, falls within the range of 2 µm to 8 µm. The electrical interference between the impacted TSVs and signal-transmitting TSVs (intense TSVs) may be evaluated using finite element analysis and a 3D IC model, as illustrated in Figure 1. Figure 1(a) shows TSVs with a single-liner structure, while Figure 1(b) presents TSVs with a stacked-liner structure. Figure 1(c) depicts the potential variation between aggressive and victim TSVs using disparate dielectric materials in a single-liner 3D IC configuration, and Figure 1(d) illustrates the corresponding potential variation in a stacked-liner 3D IC configuration. Finite element method (FEM) models draw on a wide range of physical disciplines, including electrostatics, heat transport, and many more.

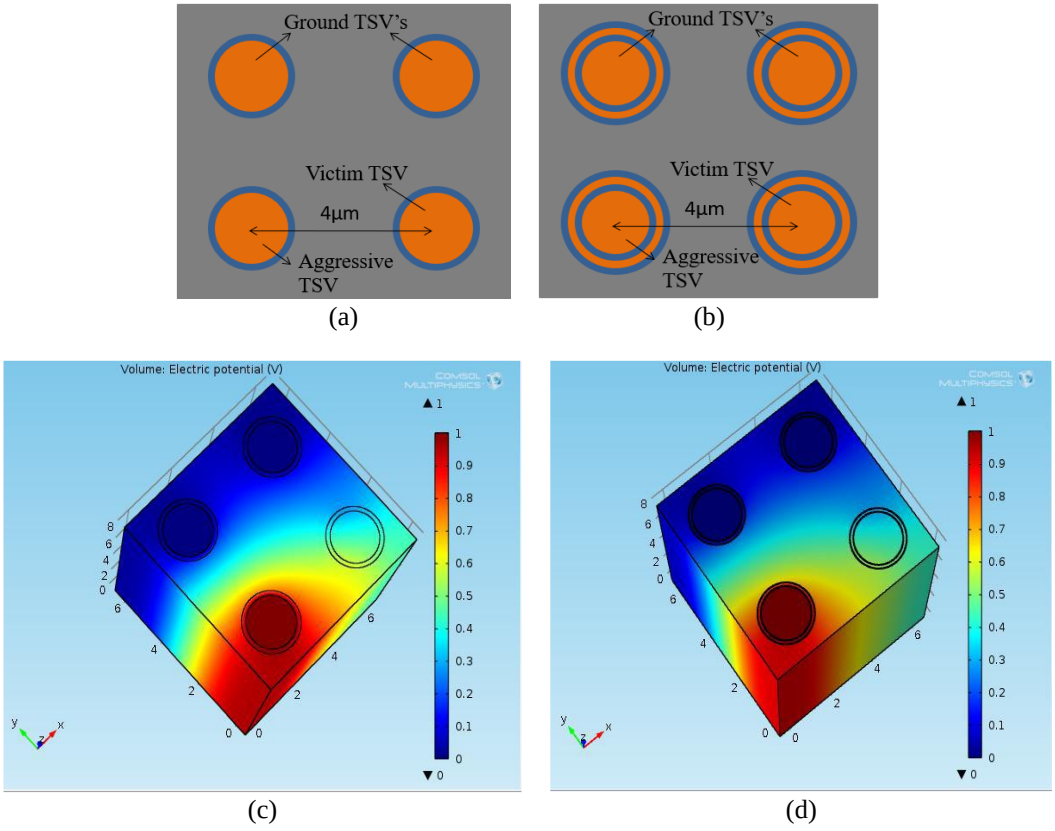

Figure 1. Top-view electrical TSV (ETSV) models illustrating different liner configurations and potential variations; (a) TSVs with single-liner structure, (b) TSVs with stacked-liner structure, (c) potential variation between aggressive and victim TSVs using disparate dielectric materials in a single-liner 3D IC configuration, and (d) potential variation between aggressive and victim TSVs using disparate dielectric materials in a stacked-liner 3D IC configuration

The TSVs have a total area of 4 µm, a thickness of 0.15 µm, and a height of 8 µm, as shown in Table 1. A wide range of dielectric materials with different ratios were included in the simulation. Teflon-AF 1600's exceptional heat stability, low dielectric loss, and low dielectric constant make it a valuable dielectric material. It works wonderfully for uses involving high frequencies and effective energy storage. It is well-

suited for high-tech electronic devices, such as flexible and wearable electronics, due to its adaptable molecular structure and compatibility with flexible substrates. Furthermore, it performs reliably over time and in a variety of environments thanks to its environmental resilience. The results reveal that compared to traditional materials, Teflon-AF 1600 has superior dielectric characteristics, resulting in a 44.4% decrease in noise coupling and a 20% reduction in power consumption. High melting point materials improve thermal stability and avoid TSV deterioration; this proves that Teflon-AF 1600 is a viable option for lowering noise coupling in 3D ICs, which in turn enables high-performance, dependable 3D ICs for a wide range of uses. Reducing hotspots is made possible by high thermal conductivity, which allows for effective heat dispersion. Taken as a whole, these features boost TSV performance and dependability.

Table 1. Simulation parameters as per ITRS roadmap

Parameter	Value
TSV diameter	2.00 µm
Liner material thickness	0.150 µm
TSV height	8.00 µm
Aggressive TSV to victim TSV distance	4.00 µm
Pitch	2.00 µm

Table 2 indicates the key physical and electrical properties of dielectric materials used in TSV liner structures. It shows that Teflon AF 1600 has the lowest dielectric constant and thermal conductivity, making it ideal for minimising capacitive coupling and heat transfer. Compared to conventional SiO_2, low-k materials such as BCB, Perylene-N, and Teflon AF 1600 offer superior electrical isolation and thermal stability for advanced 3D IC applications. Figure 1 illustrates the ETSV top-view models comparing single- and stacked-liner structures. It also depicts how the potential varies between aggressive and victim TSVs when different dielectric materials are employed in both configurations. Figure 2 illustrates the ETSV visual representation of the proposed model for single- and stacked-liner structures. Figure 3 presents a visual representation of the proposed model that evaluates clamour coupling from a top-down perspective. Figure 4 shows the stacked liner structure, where various dielectric materials are employed, and the variations between the TSVs are examined in a 3D view. Figure 5 explains the exploration of electrical interference; the dielectric properties of Teflon AF 1600 were scrutinised using a top-view ETSV model.

Table 2. Various dielectric materials used in TSVs examined

Parameter	SiO_2	BCB	Teflon AF 1600	Perylene-N
Dielectric constant (–)	3.9	2.5	1.9	2.2
Volume resistivity (Ω·cm)	$>10^{18}$	1×10^{19}	10×10^{22}-10×10^{24}	1.4×10^{17}
Melting point (°C)	>1500	350	327	420
Coefficient of thermal conductivity (W/m·K)	1.4	0.3	0.25	0.126
Coefficient of thermal expansion (ppm/°C)	0.5	42	1.2-1.7	69

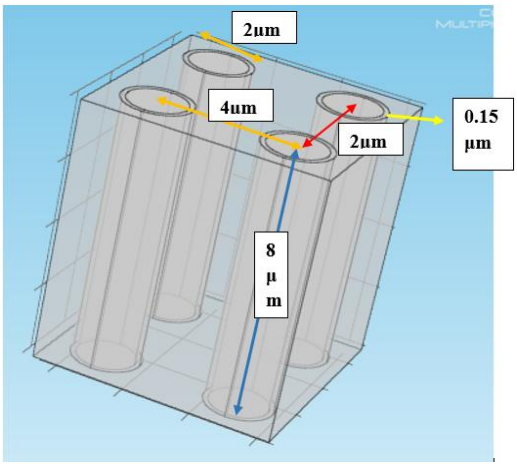

Figure 2. Suggested model visual representation

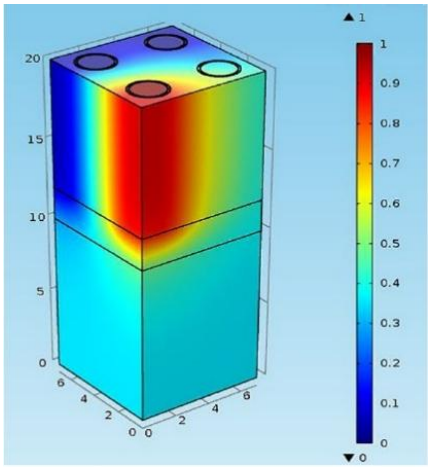

Figure 3. 3D view of a stacked liner structure and various dielectric materials

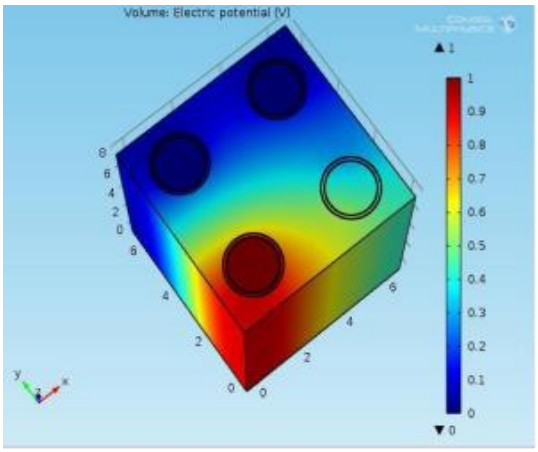

Figure 4. Top-view ETSV model with Teflon-AF 1600 dielectric characteristics

4. SIMULATION RESULTS

Reducing TSV pitch increases capacitive coupling, leading to higher crosstalk and noise. Increasing pitch improves signal isolation by reducing electromagnetic interference. Thus, TSV pitch presents a trade-off between integration density and noise performance. Explores how proposed low-k dielectrics influence electrical potential in single- and stacked-liner TSVs. By comparing Teflon AF 1600, BCB, and Perylene-N against SiO_2, the study assesses capacitive coupling, field confinement, and signal integrity across 1 GHz to 1 THz, highlighting stacked liners' superior isolation.

4.1. Electrical potential of single liner structure using proposed dielectric materials

Figures 5 and 6 show how the electric potential varies along the arc length between the aggressive TSV and the victim TSV at an operating frequency of 10 GHz for different dielectric liner materials—SiO_2, Teflon-AF 1600, BCB, and Perylene-N—in a single-liner TSV structure. Capacitive coupling between the conductive vias and the surrounding dielectric mainly causes noise coupling between TSVs. As the arc length increases to 4 μm, corresponding to the distance between the aggressive and victim TSVs, the electric potential gradually decreases for all materials. This decrease suggests that increasing the pitch between TSVs effectively reduces capacitive coupling, thereby suppressing noise interference.

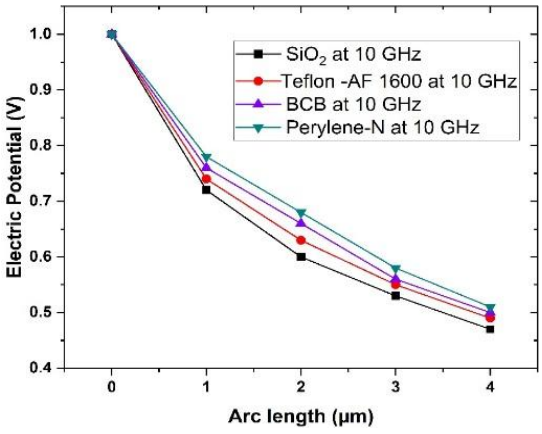

Figure 5. Electric potential variation along the arc between aggressor and victim TSVs for various dielectrics (SiO_2, BCB, Perylene-N, and Teflon AF 1600) in a single-liner TSV at 10 GHz

Figure 5 shows that among the investigated dielectric materials, SiO_2 exhibits the lowest electric potential at 4 μm, indicating superior insulation at this distance. Compared with low-k materials such as BCB, Perylene-N, and Teflon-AF 1600, SiO_2 achieves approximately 7.8% noise reduction and 6.56 dB signal attenuation at the victim TSV position. Although low-k materials generally reduce capacitive coupling

more effectively, in this specific configuration and frequency, SiO_2 demonstrates better suppression of cross-coupled noise due to its comparatively stable dielectric behaviour and higher breakdown voltage strength. Figure 6 shows that among the tested dielectric materials, Teflon AF 1600 has the lowest electric potential at a spacing of 4 μm, indicating its superior isolation performance at this distance. Compared to other low-k materials such as BCB, Perylene-N, and SiO_2, Teflon AF 1600 achieves about 35.3% noise reduction and 9.63 dB signal attenuation at the victim TSV location compared to conventional SiO_2. Although low-k materials generally provide more effective capacitive coupling reduction, Teflon AF 1600 demonstrates better suppression of cross-coupled noise in this setup and frequency range, due to its stable dielectric properties and higher breakdown strength in a single-liner structure at 1 THz.

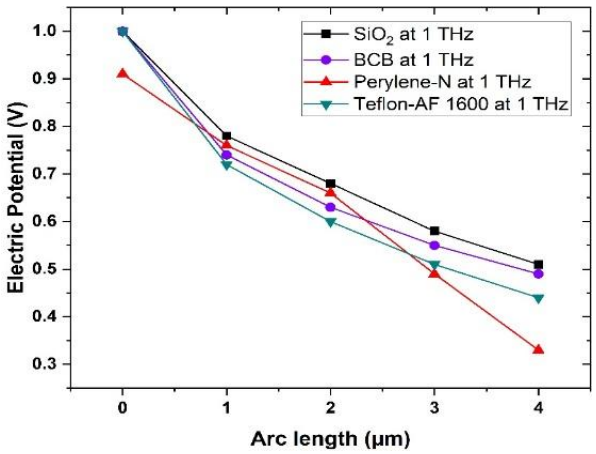

Figure 6. Electric potential variation along the arc between aggressor and victim TSVs for various dielectrics (SiO_2, BCB, Perylene-N, and Teflon AF 1600) in a single-liner TSV at 1 THz

4.2. Electrical potential of stacked liner structure using proposed dielectric materials

Figures 7 and 8 show how the electric potential varies along the arc length between the aggressive TSV and the victim TSV at an operating frequency of 10 GHz for different dielectric liner materials—SiO_2, Teflon-AF 1600, BCB, and Perylene-N—in a stacked-liner TSV structure. Capacitive coupling between the conductive vias and the surrounding dielectric mainly causes noise coupling between TSVs. As the arc length increases to 4 μm, corresponding to the distance between the aggressive and victim TSVs, the electric potential gradually decreases for all materials. This decrease suggests that increasing the pitch between TSVs effectively reduces capacitive coupling, thereby suppressing noise interference.

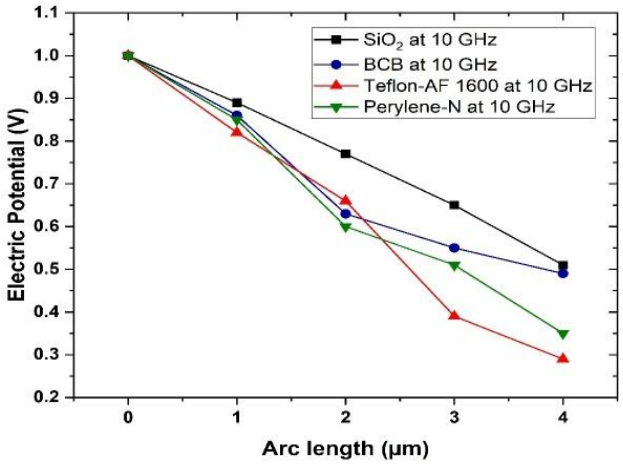

Figure 7. Electric potential variation along the arc between aggressor and victim TSVs for various dielectrics (SiO_2, BCB, Perylene-N, and Teflon AF 1600) in a stacked-liner TSV at 10 GHz

Figure 7 shows that among the tested dielectric materials, Teflon AF 1600 has the lowest electric potential at a spacing of 4 μm, indicating its superior isolation performance at this distance. Compared to other low-k materials such as BCB, Perylene-N, and SiO_2, Teflon AF 1600 achieves about 33.5% noise reduction and 10.46 dB signal attenuation at the victim TSV location compared to conventional SiO_2. Although low-k materials generally provide more effective capacitive coupling reduction, Teflon AF 1600 demonstrates better suppression of cross-coupled noise in this setup and frequency range, due to its stable dielectric properties and higher breakdown strength for a stacked liner structure at 10 GHz.

Figure 8 shows that among the tested dielectric materials, Teflon AF 1600 has the lowest electric potential at a spacing of 4 μm, indicating its superior isolation performance at this distance. Compared to other low-k materials such as BCB, Perylene-N, and SiO_2, Teflon AF 1600 achieves about 44.4% noise reduction and 12.04 dB signal attenuation at the victim TSV location compared to conventional SiO_2. Although low-k materials generally provide more effective capacitive coupling reduction, Teflon AF 1600 demonstrates better suppression of cross-coupled noise in this setup and frequency range, due to its stable dielectric properties and higher breakdown strength for a stacked liner structure at 1 THz.

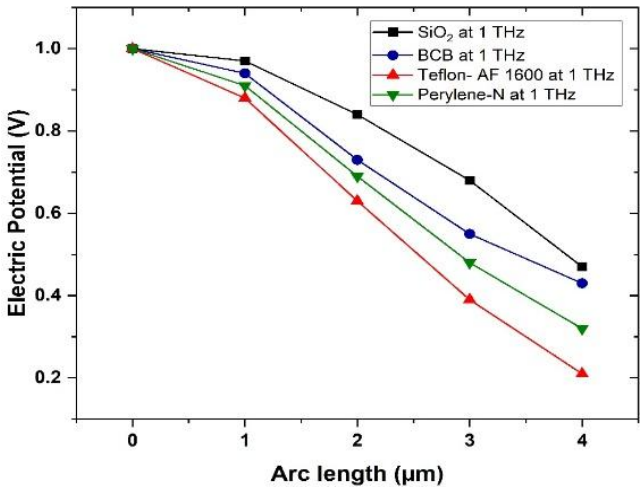

Figure 8. Electric potential variation along the arc between aggressor and victim TSVs for various dielectrics (SiO_2, BCB, Perylene-N, and Teflon AF 1600) in a stacked-liner TSV at 1 THz

5. CONCLUSION

The study on reducing noise coupling in 3D ICs through dielectric liner selection highlights clear advantages for low-k materials — namely, Teflon AF 1600, BCB, and Perylene-N — over Sio_2. The study is primarily simulation-based with limited experimental validation. It considers a restricted set of dielectric materials and idealized TSV structures.Thermal–electrical coupling and large-scale TSV array effects are not fully explored. Analysing single-liner and stacked-liner Through-Silicon Via structures from 1 GHz to 1 THz shows that dielectric selection significantly influences capacitive coupling and signal integrity. At 10 GHz, a single-liner with SiO_2 provides only modest noise reduction, whereas stacked-liner configurations with Teflon AF 1600 yield substantial enhancements, achieving a 33.3% noise reduction and an 8.40 dB attenuation. At 1 THz, the benefits of Teflon AF 1600 are even more apparent, with up to 44.4% noise reduction and a 12.04 dB decrease in attenuation in stacked-liner layouts. These results suggest that stacked-liner TSVs with optimised dielectric layering offer superior isolation and field confinement, outperforming single-liner designs. Overall, low-k dielectrics, especially Teflon AF 1600, prove to be highly effective isolation materials for 3D ICs, improving signal integrity by reducing capacitive coupling and crosstalk. Teflon AF 1600 consistently delivers better noise suppression and attenuation across various configurations, highlighting its potential for next-generation high-frequency 3D integration.

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Name of Author	C	M	So	Va	Fo	I	R	D	O	E	Vi	Su	P	Fu
Pathakunta Guru Prathap Reddy	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓			✓
Sravan Abhilash Kothapalli		✓		✓	✓		✓			✓	✓	✓	✓	

C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

The authors declare that they have no conflict of interest regarding the publication of this paper.

ETHICAL APPROVAL

This article does not contain any studies with human or animal subjects.

DATA AVAILABILITY

Data availability is not applicable to this paper as no new data were created or analyzed in this study.

REFERENCES

[1] D. Pragathi *et al.*, "Simplistic approach to alleviate noise coupling issues in 3D IC integration," *Materials Today: Proceedings*, vol. 33, pp. 4007–4011, 2020, doi: 10.1016/j.matpr.2020.06.380.

[2] Z. Zhao *et al.*, "Electrical characterization of through-silicon-via-based coaxial line for high-frequency 3D integration (invited paper)," *Electronics*, vol. 11, no. 20, p. 3417, Oct. 2022, doi: 10.3390/electronics11203417.

[3] X. Liu, Z. Zhu, Y. Yang, F. Wang, and R. Ding, "Reduction of signal reflection in high-frequency three-dimensional (3D) integration circuits," *IEICE Electronics Express*, vol. 10, no. 14, pp. 20130449–20130449, 2013, doi: 10.1587/elex.10.20130449.

[4] B. Wu and H. Wang, "Methods and designs for improving the signal integrity for 3D electrical interconnects in high performance IC packaging," in *2011 IEEE Electrical Design of Advanced Packaging and Systems Symposium (EDAPS)*, IEEE, Dec. 2011, pp. 1–4, doi: 10.1109/EDAPS.2011.6213775.

[5] S. M. S. Harb and W. Eisenstadt, "Signal integrity in high speed 3D IC design: A case study," in *2021 IEEE Nordic Circuits and Systems Conference (NorCAS)*, IEEE, Oct. 2021, pp. 1–5, doi: 10.1109/NorCAS53631.2021.9599649.

[6] D. Pragathi, N. A. Vignesh, C. U. Kumari, T. Padma, and A. K. Panigrahy, "Noise performance improvement in future IC integration using perylene-N as dielectric material," *International Journal of Innovative Technology and Exploring Engineering*, vol. 9, no. 2, pp. 1056–1059, Dec. 2019, doi: 10.35940/ijitee.L2620.129219.

[7] J. U. Knickerbocker *et al.*, "3-D silicon integration and silicon packaging technology using silicon through-vias," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 8, pp. 1718–1725, Aug. 2006, doi: 10.1109/JSSC.2006.877252.

[8] R. Vempalle and P. K. Dhal, "Loss minimization by reconfiguration along with distributed generator placement at radial distribution system with hybrid optimization techniques," *Technology and Economics of Smart Grids and Sustainable Energy*, vol. 5, no. 1, p. 18, Dec. 2020, doi: 10.1007/s40866-020-00088-2.

[9] A. Todri, S. Kundu, P. Girard, A. Bosio, L. Dilillo, and A. Virazel, "A study of tapered 3-D TSVs for power and thermal integrity," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 21, no. 2, pp. 306–319, Feb. 2013, doi: 10.1109/TVLSI.2012.2187081.

[10] V. Sundaram, Q. Chen, Y. Suzuki, G. Kumar, F. Liu, and R. Tummala, "Low-cost and low-loss 3D silicon interposer for high bandwidth logic-to-memory interconnections without TSV in the logic IC," in *2012 IEEE 62nd Electronic Components and Technology Conference*, IEEE, May 2012, pp. 292–297, doi: 10.1109/ECTC.2012.6248844.

[11] D. H. Kim, S. Kim, and S. K. Lim, "Impact of nano-scale through-silicon vias on the quality of today and future 3D IC designs," in *International Workshop on System Level Interconnect Prediction*, IEEE, Jun. 2011, pp. 1–8, doi: 10.1109/SLIP.2011.6135435.

[12] J. Wang *et al.*, "A short review of through-silicon via (TSV) interconnects: Metrology and analysis," *Applied Sciences*, vol. 13, no. 14, p. 8301, Jul. 2023, doi: 10.3390/app13148301.

[13] H. Wang, M. H. Asgari, and E. Salman, "Compact model to efficiently characterize TSV-to-transistor noise coupling in 3D ICs," *Integration*, vol. 47, no. 3, pp. 296–306, Jun. 2014, doi: 10.1016/j.vlsi.2013.10.006.

[14] K. Yoon *et al.*, "Modeling and analysis of coupling between TSVs, metal, and RDL interconnects in TSV-based 3D IC with silicon interposer," in *2009 11th Electronics Packaging Technology Conference*, IEEE, Dec. 2009, pp. 702–706, doi: 10.1109/EPTC.2009.5416458.

[15] J. Kim, J. Cho, and J. Kim, "TSV modeling and noise coupling in 3D IC," in *3rd Electronics System Integration Technology Conference ESTC*, IEEE, Sep. 2010, pp. 1–6, doi: 10.1109/ESTC.2010.5642967.

[16] V. Rafi, P. K. Dhal, S. H. Vali, S. R. Krishna, U. Suryavalli, and S. V. J. Prakash, "Enhanced multi-mode control of Z-source virtual synchronous generator for photovoltaic systems using fuzzy logic controller," *International Journal of Applied Power Engineering (IJAPE)*, vol. 14, no. 3, pp. 701–711, Sep. 2025, doi: 10.11591/ijape.v14.i3.pp701-711.
[17] J. Cho *et al.*, "Modeling and analysis of through-silicon via (TSV) noise coupling and suppression using a guard ring," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 1, no. 2, pp. 220–233, 2011, doi: 10.1109/TCPMT.2010.2101892.
[18] X. Gu, J. Silberman, Y. Liu, and X. Duan, "Mitigating TSV-induced substrate noise coupling in 3-D IC using buried interface contacts," in *2012 IEEE 21st Conference on Electrical Performance of Electronic Packaging and Systems*, IEEE, Oct. 2012, pp. 75–78, doi: 10.1109/EPEPS.2012.6457846.
[19] A. E. Engin and S. R. Narasimhan, "Modeling of crosstalk in through silicon vias," *IEEE Transactions on Electromagnetic Compatibility*, vol. 55, no. 1, pp. 149–158, 2013, doi: 10.1109/TEMC.2012.2206816.
[20] C. Xue, Z. Cheng, Z. Chen, Y. Yan, Z. Cai, and Y. Ding, "Elimination of scallop-induced stress fluctuation on through-silicon-vias (TSVs) by employing polyimide liner," *IEEE Transactions on Device and Materials Reliability*, vol. 18, no. 2, pp. 266–272, 2018, doi: 10.1109/TDMR.2018.2826557.
[21] R. Vempalle and P. K. Dhal, "Optimal analysis of time varying load radial distribution system with photovoltaic and wind generating system using novel hybrid optimization technique," *Renewable Energy Focus*, vol. 41, pp. 246–257, Jun. 2022, doi: 10.1016/j.ref.2022.03.004.
[22] M. Jung, J. Mitra, D. Z. Pan, and S. K. Lim, "TSV stress-aware full-chip mechanical reliability analysis and optimization for 3D IC," *Communications of the ACM*, vol. 57, no. 1, pp. 107–115, 2014, doi: 10.1145/2494536.
[23] V. Rafi, P. K. Dhal, M. Rajesh, D. R. Srinivasan, M. Chandrashekhar, and N. M. Reddy, "Optimal placement of time-varying distributed generators by using crow search and black widow - Hybrid optimization," *Measurement: Sensors*, vol. 30, p. 100900, Dec. 2023, doi: 10.1016/j.measen.2023.100900.
[24] S. Zhong, S. Wang, Q. Chen, and Y. Ding, "Thermal reliability analysis and optimization of polymer insulating through-silicon-vias (TSVs) for 3D integration," *Science China Technological Sciences*, vol. 57, no. 1, pp. 128–135, Jan. 2014, doi: 10.1007/s11431-013-5409-9.
[25] M. Chandrakar and M. K. Majumder, "Effect of polymer liners in different via shapes: impact on crosstalk induced delay," *Research Square PrePrint*, 2021, [Online]. Available: https://doi.org/10.21203/rs.3.rs-1147569/v1
[26] J. M. Kim, M. S. Kim, and M. M. Hussain, "From 3D-IC to 3D-HI for environmentally durable rugged electronics (EnDuRE)," *IEEE Electron Devices Reviews*, vol. 1, pp. 31–52, Oct. 2024, doi: 10.1109/EDR.2024.3491714.

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